Two-phase low-power analog CMOS
Peak detector with high dynamic range
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Abstract
A low-power two-phase peak detector with wide dynamic range was developed. The PD was designed on the basis of the CMOS UMC 180 nm process. This block is considered as a part of the read-out electronics of the CBM experiment at the FAIR accelerator (Germany). Peak detector has the following advantages: wide dynamic range of 5 - 1000 mV, low power consumption of 500 µW. The designed PD meets the requirements to the muon chamber read-out electronics of the CBM experiment. Due to the area efficiency (100 x 90 µm²) and low power consumption it can be used in different applications for high-energy physics read-out electronics.

Peak detector specifications
In the multi-channel detector read-out systems the two-phase configuration is usually applicable. In this configuration the drawbacks of the classical PD structure are eliminated. In particular, the two-phase configuration has the following advantages:
• Absence of the input offset voltage (i.e. the accuracy is not limited by the input offset voltage of the OpAmp);
• Common-mode errors have no influence on the accuracy;
• The influence of the input transistors process mismatch is decreased.

Schematics
The main block of the two-phase PD is the OTA (Figure 3). That amplifier corresponds to the requirements on power consumption and dynamic range. The OTA is optimized for the operation with negative polarity signals with amplitudes in the range of 5 - 500 mV.

Operational transconductance amplifier
This schematic consists of the OTA, rectifying current mirror, hold capacitor, reset scheme, -Peak Find- signal scheme, and analog gates to switch between the “read” and “write” phases.

Peak detector schematic

Functionality diagram
PD transfer function
Distribution of the output peak value

Specifications
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
<th>Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input signal dynamic range, mV</td>
<td>5 - 500</td>
<td>5 - 1000</td>
</tr>
<tr>
<td>Die size, µm²</td>
<td>100 x 150</td>
<td>100 x 90</td>
</tr>
<tr>
<td>Regular occupancy, MHz</td>
<td>0.3</td>
<td>0.4</td>
</tr>
<tr>
<td>Power consumption, mW</td>
<td>1</td>
<td>0.55</td>
</tr>
</tbody>
</table>

Conclusions and outlooks
The low-power analog peak detector with a wide dynamic range for readout electronics for the muon chambers of the CBM experiment was designed. It was developed on the basis of the UMC 180 nm CMOS process. The peak detector meets the requirements to the readout electronics for the muon chambers of the CBM experiment.

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