Two-phase low-power analog CMOS Peak detector with high dynamic range

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Abstract

A low-power two-phase peak detector with wide dynamic range was developed. The PD was designed on the basis of the CMOS UMC 180 nm process. This block is considered as a part of the read-out electronics of the CBM experiment at upcoming FAIR accelerator (Germany). Peak detector has the following advantages: wide dynamic range of 5 - 1000 mV, low power consumption of 500 μW. The designed PD meets the requirements to the muon chamber read-out electronics of the CBM experiment. Due to the area efficiency (100 x 90 μm^2) and low power consumption it can be used in different applications for high-energy physics read-out electronics.

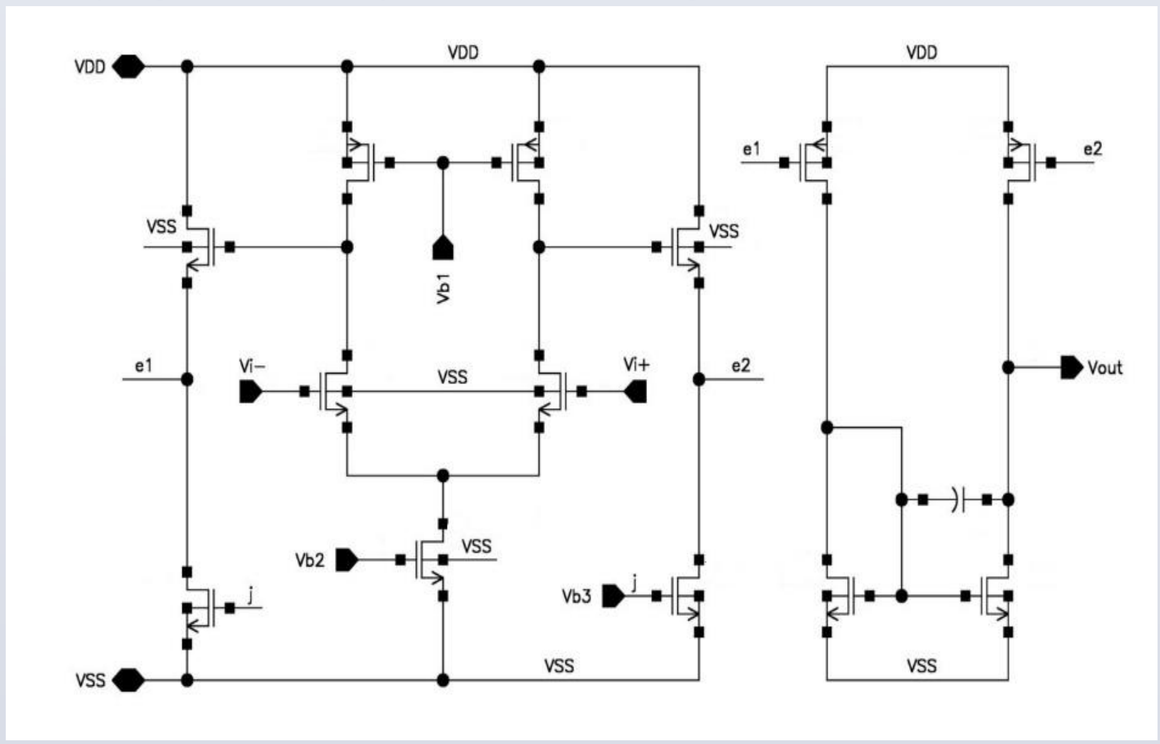
Peak detector specifications

In the multi-channel detector read-out systems the two-phase configuration is usually applicable. In this configuration the drawbacks of the classical PD structure are eliminated. In particular, the two-phase configuration has the following advantages:

- Absence of the input offset voltage (i.e. the accuracy is not limited by the input offset voltage of the OpAmp);
- Common-mode errors have no influence on the accuracy;
- The influence of the input transistors process mismatch is decreased.

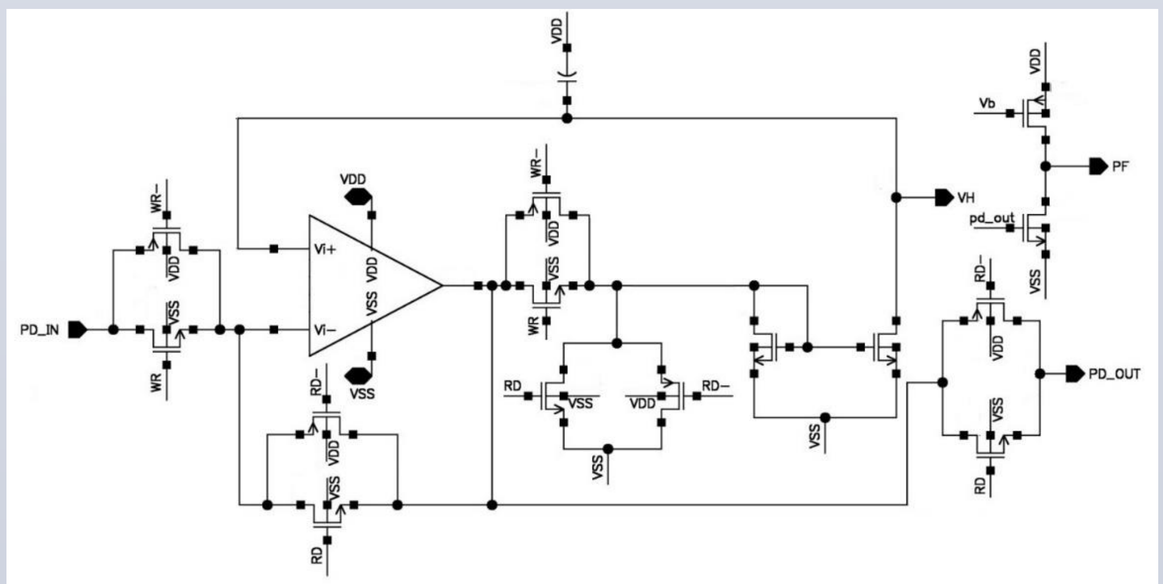
Schematics

The main block of the two-phase PD is the OTA (Figure 3). That amplifier corresponds to the requirements on power consumption and dynamic range. The OTA is optimized for the operation with negative polarity signals with amplitudes in the range of 5 – 500 mV.

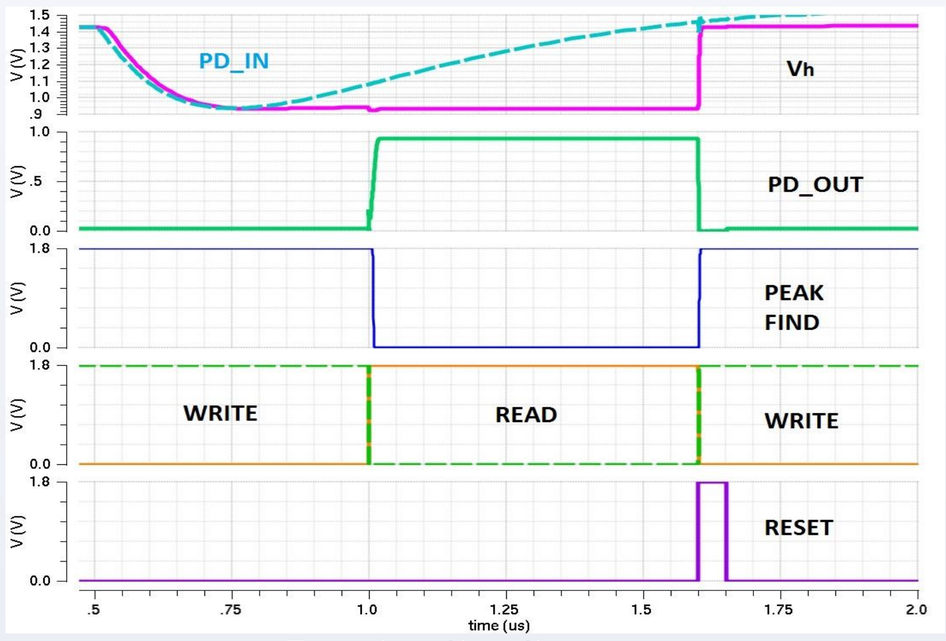


Operational transconductance amplifier

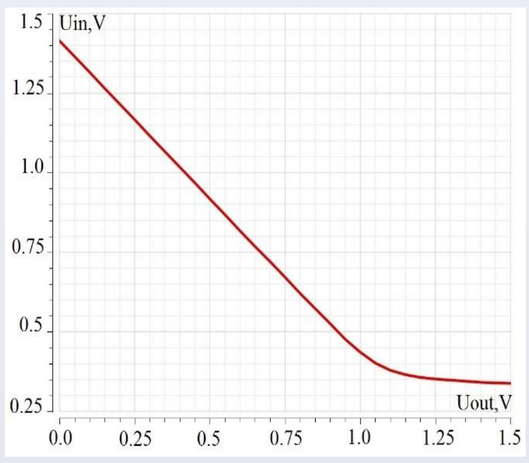
This schematic consists of the OTA, rectifying current mirror, hold capacitor, reset scheme, «Peak Find» signal scheme, and analog gates to switch between the "read" and "write" phases.



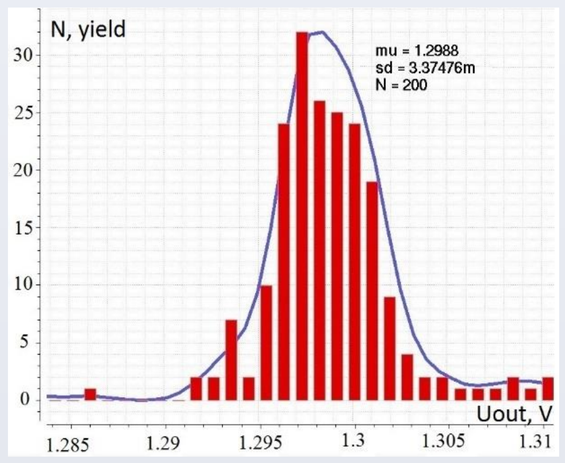
Peak detector schematic



Functionality diagram

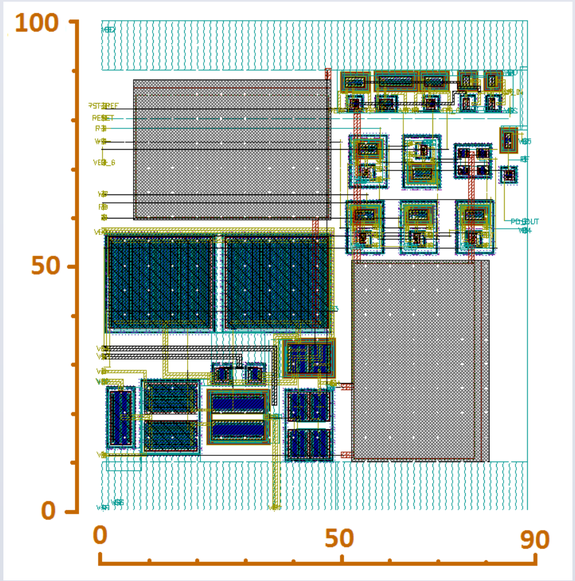


PD transfer function



Distribution of the output peak value

Peak detector specifications



The PD layout (Figure 8) was designed according to the UMC 180 nm process rules. The area of the Peak Detector is 100 x 90 μm^2. Here the 100 μm - is the height of the peak detector, which is in correspondence to the analog channel height standard in the read-out electronics for the muon system of the CBM experiment.

Specifications

Parameter	Specification	Simulation
Input signal dynamic range, mV	5 -500	5 - 1000
Die size, μm^2	100 x 150	100 x 90
Regular occupancy, MHz	0.3	0.4
Power consumption, mW	1	0.55

Conclusions and outlooks

The low-power analog peak detector with a wide dynamic range for readout electronics for the muon chambers of the CBM experiment was designed. It was developed on the basis of the UMC 180 nm MMRF CMOS process. The peak detector meets the requirements to the readout electronics for the muon chambers of the CBM experiment.

Acknowledgments

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