

Two-phase low-power analog CMOS Peak detector with high dynamic range

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A low-power two-phase peak detector with wide dynamic range was developed. The PD was designed on the basis of CMOS UMC 180 nm process. This block is considered as a part of the read-out electronics of the CBM experiment at upcoming FAIR accelerator (Germany). Peak detector has the following advantages: wide dynamic range of 5 - 1000 mV, low power consumption of 500 uW. The designed PD meets the requirements to the read-out electronics of the CBM experiment muon chamber. Due to the area efficiency (100 x 90 μm^2) and low power consumption it can be used in the different applications for high-energy physics read-out electronics.

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