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High Speed SLVS Transmitter and Receiver

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Design of SLVS chip-to-chip communication transmitter/receiver IP block in 180 nm UMC MMRF CMOS process is presented. This block has been developed for study a data transmission over PCBs and/or electrical cables (lines) of few meters length at rates up to 320 Mb/s. Schematic for on-chip testing is also presented. This blocks is used for communication between front-end ASICs and DAQ system.

Presentation type

Section talk (10+5 min)

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