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Asynchronous data readout system for multichannel ASIC

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Data readout system of multichannel data-driven ASIC, requiring high-speed (320 Mb/s) output data serialization is described. Its structure, based on a limited number of FIFO blocks, provides a lossless data transfer. The solution has been realized as a separate test IP block in the prototyped 8 channel ASIC, intended for muon chamber of CBM experiment at FAIR. The block was developed in the UMC 0.18 um MMRF CMOS process and prototyped via Europractice. Main parameters of the chip are given.

Presentation type

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