Contribution ID : **90** Type : **not specified**

Development of the Read-out ASIC for Muon Chambers

Saturday, 10 October 2015 10:00 (15)

A front-end prototype ASIC for muon chambers is presented. ASIC was designed and prototyped in CMOS UMC MMRF 180 nm process via Europractice. The chip includes 8 analog processing channels, each consisting of preamplifier, two shapers (fast and slow),differential comparator and an area efficient 6 bit SAR ADC with 1.2 mW power consunption at 50 Msps. The chip also includes the threshold DAC and digital serializer. The design has the following features: dynamic range of 100 fC, channel hit rate of 2 MHz, ENC of 1000 e- at 50 pF, power comsumption of 10 mW per channel, 6 bit SAR ADC.

Presentation type

Section talk (10+5 min)

Primary author(s) : Mr. EVGENY, Malankin (NRNU MEPHI)

Co-author(s) : Mr. GUSEV, Alexander (NRNU MEPhI); Dr. VORONIN, Alexander (SINP MSU); Mr. NORMANOV, Dmitry (NRNU Mephi); Dr. ATKIN, Eduard (National Research Nuclear University MEPhI); Mr. SAGDIEV, Ilias (NRNU MEPhI); Mr. BULBAKOV, Ivan (NRNU MEPhI); Mr. SHUMKIN, Oleg (NRNU MEPhI); Mr. IVANOV, Pavel (NRNU MEPhI); Mr. VINOGRADOV, Sergey (NRNU MEPhI); Mr. SHUMIKHIN, Vitaly (NRNU MEPhI)

Presenter(s) : Mr. EVGENY, Malankin (NRNU MEPHI)

Session Classification : Methods of experimental physics - parallel V

Track Classification : Methods of experimental physics