Multichannel readout ASIC design flow for high energy physics and cosmic rays experiments

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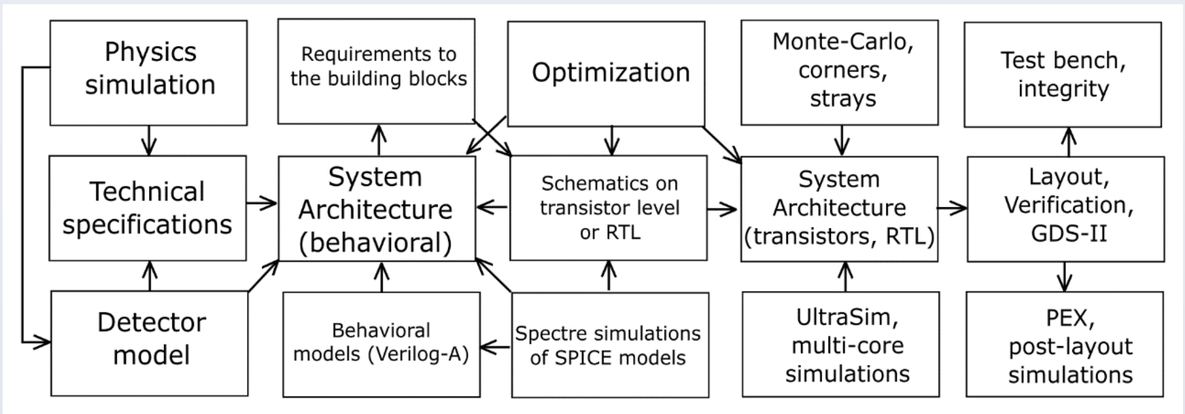
Abstract

In the large-scale high energy physics and astrophysics experiments multi-channel readout application specific integrated circuits (ASICs) are widely used. The ASICs for such experiments are complicated systems, which usually include both analog and digital building blocks. The complexity and large number of channels in such ASICs require the proper methodological approach to their design. The paper represents the mixed-signal design flow of the ASICs for high energy physics and cosmic rays experiments. This flow was successfully embedded to the development of the read-out ASIC prototype for the muon chambers of the CBM experiment. The approach was approved in UMC CMOS MMRF 180 nm process. The design flow enable to analyse the mixed-signal system operation on the different levels: functional, behavioural, schematic and post layout including parasitic elements. The proposed design flow allows reducing the simulation period and eliminating the functionality mismatches on the very early stage of the design.

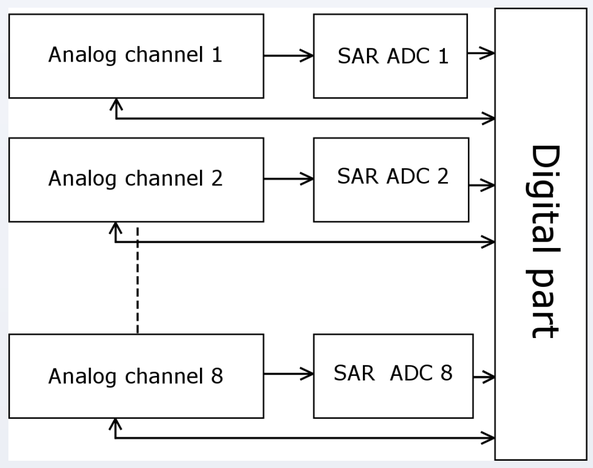
ASIC design approach for HEP and Space experiments



Design flow of mixed-signal ASIC for HEP and cosmic rays experiments

- **Technical specifications** arise from the physics simulations (e.g. GEANT). Then, using the detector model, it is determined the specifications of electronics (number of channels, power consumption, rate, dynamic range, etc.).
- **Behavioral system architecture** is based on technical specifications, physics and detector simulation. Architecture should be simulated on the virtual elements (e.g. Verilog-A) using Cadence tool set. On the platform of the first virtual models the specifications of the building blocks are established in general.
- **Simulations in SPICE environment with SPECTRE simulator** give the most adequate approach to the real device That framework allows carrying out the mixed-signal simulation in the single environment, at the same time giving the number of parameters, taking into account the schematic non-idealities and determining the critical parameters of the schematics.
- **Building blocks designed on the transistor level or as RTL** replace the correspondent behavioral part in the system model. When the behavioral block model is changed to the real one, the comparison of the parameters is carried out, as well as the simulation of mismatches in load capacity, signal polarity, time diagrams and etc.
- **Verification of the layouts** is necessary to fix the design rules errors and the mismatches between the schematic and layout (DRC and LVS). The parasitic extraction (PEX), inclusion of the package and PCB stray elements, post layout simulations are another important step in the ASIC design. Those simulations can give the best approach of the project to the real conditions. This stage is characterized by the following types of the analysis and simulations:
  a) simulations with the extracted parasitic elements;
  b) Monte-Carlo simulation of the process variations;
  c) Simulation of the process corners;
  d) temperature variations;
  e) IR-drops on wires in the whole area of the die;
  f) gate delays simulations;
  g) integrity (signal transfer either inside the chip and on the PCB).

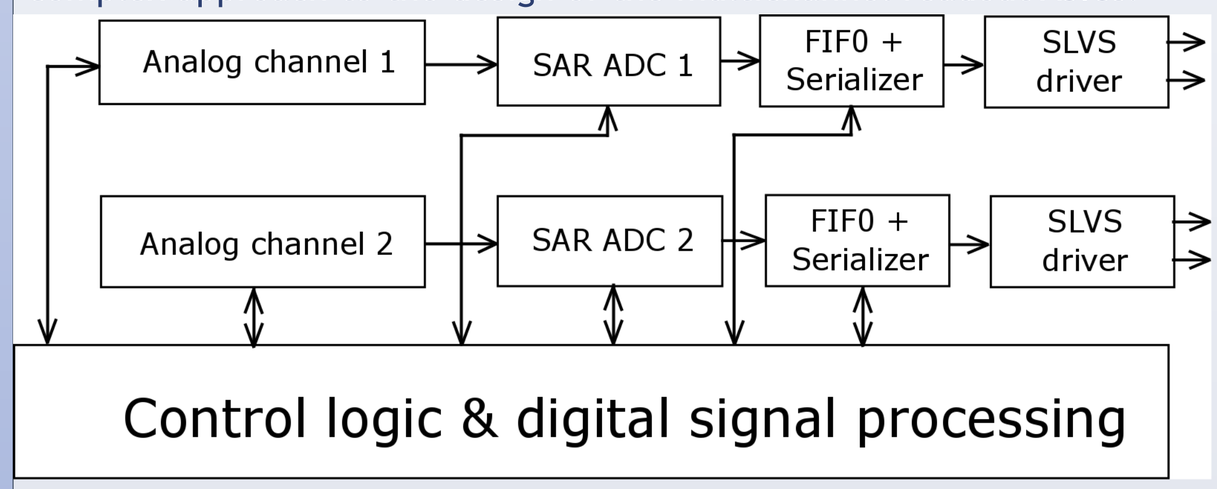
Approbation of the design approach



8-channel prototype ASIC structure

The ASIC was designed according to the classical approach of bottom-to-top design flow. The experimental studies of the chip showed that the ADC is non-operable. The reason of it was in the mismatch of the signal polarity in the unit starting the ADC conversion. Thus, it becomes impossible to obtain the digitized information from the channels.

This kind of mistake could be eliminated by the application of the complex approach to the design of the multichannel readout ASICs.



2-channel mixed-signal prototype ASIC structure, designed with proposed flow

The next prototype includes is a part of the full readout system of the up-to-date HEP and space experiments.

The behavioral model of the channel was designed using the Verilog-A models (e.g. amplifiers, ADC, DAC and etc.). The digital part of the channel which controls the ADC operation, as well as the channel memory (FIFO) and serializer were designed with the Verilog-A models. These allow simulating the full mixed-signal system functionality. Then the Verilog-A models were replaced by the real transistor blocks seriously.

The digital schematic is based on the special standard cell library of the UMC 180 nm process. The library includes the schematic equivalent of the RTL digital part design. Thus, the mixed-signal system was designed and it was possible to simulate in the analog environment (single simulation environment). Thus, it was fixed all the mismatches between the analog signal as particularly polarities and delays. To realize this design flow the most of the Cadence tools as ADE, ADE XL (Monte-Carlo and Corners), simulation accelerating options (APS and XPS), and calculating algorithms were used.

Summary

The readout ASIC design top-to-bottom-to-top serial flow for HEP and cosmic rays experiments was described. The design flow makes possible to analyze the mixed-signal system operation on the different levels: functional, behavioral, schematic and post layout including parasitic elements. The proposed design flow allows reducing the simulation period and eliminating the functionality mismatches on the very early stage of the design. It was successfully embedded to the development of the read-out ASIC prototype for the muon chambers of the CBM experiment. The approach was approved in UMC CMOS MMRF 180 nm process.

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