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A Low jitter All - Digital Phase - Locked Loop in 180 nm CMOS technology

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Abstract — An all-digital phase-locked loop (ADPLL) was implemented in 180 nm CMOS technology. The proposed ADPLL uses a novel digitally controlled oscillator to achieve 1 ps resolution. The pure digital phase locked loop is attractive because it is less sensitive to noise and operating conditions than its analog counterpart. The proposed ADPLL can be easily ported to different process as a soft IP block, making it very suitable for system-on-chip applications.

Presentation type

Poster

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