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Creating a parameterized model of a CMOS transistor with a gate of enclosed layuot.

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We consider the method of creating a parametrized Space model of an N-channel transistor with a gate of enclosed layuot. This model provide an increased radiation tolerance. Formulas and examples of engineering calculation for the operation of models in the computer-aided Design environment of Cadence Vitruoso. Calculations are made for the CMOS technology with 180 nm design rules of the UMC.

Presentation type

Poster

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