

Creating a parameterized model of a CMOS transistor with a gate of enclosed layout.

Saturday, 10 October 2015 09:30 (30)

We consider the method of creating a parametrized Space model of an N-channel transistor with a gate of enclosed layout. This model provide an increased radiation tolerance. Formulas and examples of engineering calculation for the operation of models in the computer-aided Design environment of Cadence Virtuoso. Calculations are made for the CMOS technology with 180 nm design rules of the UMC.

Presentation type

Poster

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Session Classification : Poster session V

Track Classification : Methods of experimental physics