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Architecture of the multichannel data-driven ASIC

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The development architecture of a multichannel data-driven ASIC is presented. It provides the selection of useful events at an early stage of reading out detector signals. The architecture is based on fast cross-point switches of analog signals, followed by their digitization by a limited set of ADCs and high-speed output data serialization. Such approach reduces the number of subsequent ADCs as well as digital processing channels. That leads to lower power consumption and chip area. The results of a prototype ASIC development, based on this architecture and intended for the CBM experiment at FAIR, are given.

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