ASIC DESIGN FOR PARTICLE PHYSICS AND ASTROPHYSICS

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Abstract

- ASICs are one of the key complex technologies available to detector designers.
- ASICs are essential for integration scale, low power dissipation, high speed capability, radiation tolerance.
- For future experiments in the intensity, cosmic, and energy frontiers, ASICs should provide a new level of functionality at a new set of constraints and trade-offs, like low-noise high-dynamic range amplification and pulse shaping, high-speed waveform sampling, low power digitization, fast digital data processing, serialization and data transmission.
- All chips should allow minute almost 3D assemblies.
- The talk presents an overview of the state of the art and trends in nowadays chip design, basing partially on our ASIC lab experience.
Trend: \( N(x) = A \times \exp(t/\tau) \), \( \tau \sim 18 \) months
Cost per transistor

Intel 14 nm Continues to Deliver Lower Cost per Transistor
### Roadmap

<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>Technology Node [nm]</td>
<td>90</td>
<td>65</td>
<td>45</td>
<td>32</td>
<td>22</td>
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<tr>
<td>Transistor count [Mtr]</td>
<td></td>
<td></td>
<td>1500</td>
<td>3092</td>
<td>6184</td>
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<tr>
<td>Transistor Density [Mtr/cm²]</td>
<td>77</td>
<td>154</td>
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<tr>
<td>Chip Size</td>
<td>140</td>
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<td>Clock freq [GHz]</td>
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<td>Vdd</td>
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<td>DRAM half pitch</td>
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<td>Signal IO Pads</td>
<td>512</td>
<td>1024</td>
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<tr>
<td>Power Pads</td>
<td>1024</td>
<td></td>
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</table>

*International Technology Roadmap for Semiconductors*
CMOS technology has followed Moore’s Law for 50 years, shrinking devices and interconnect to smaller and smaller dimensions, with many technological tricks and challenges to achieve this in the transistors, the lithography and the metallization.

In 2011 Intel made a significant innovation of the first 22nm 3-D tri-gate silicon transistors. Instead of a thinner dielectric, transistors were redesigned with wider dielectric layers that surround a fin shape. This improves the control of electric field, reduce current densities and leakage, and diminish process variations.
More than Moore

Functional **diversification**: Incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law", but provide additional value in different ways.

The approach allows for the non-digital functionalities to migrate from the system board-level into the package (SiP) or onto the chip (SoC).

More than Moore

- FinFet
- Fully Depleted SOI
- Through-silicon via
- Wafer-to-wafer stacking
- Truly 3D monolithic CMOS
- New materials (III-IV, Ge, GaN, SiC, etc.)
- New phenomena: non $kT/q$ controlled thresholds slopes
- …
More than Moore: Diversification

- Analog/RF
- Passives
- HV Power
- Sensors Actuators [e.g. MEMS]
- Biochips

Interacting with people and environment
Non-digital content System-in-package (SiP)
Information processing
Digital content System-on-chip (SoC)
Combining SoC and SiP: Higher-value systems

More Moore: Miniaturization
Baseline CMOS: CPU, memory, logic
Beyond CMOS

International technology roadmap for semiconductors, 2012 Update Overview
Each strip corresponds to a separate ASIC project

No correlation between the number of prototype cycles and the number of ASICs needed

CMS

~1 000 000 custom chips (of 20 types)

Compact Muon Solenoid

A. Marchioro / CERN
- The increasing quantity of elements at a simultaneous increase in their complexity and density. Moore law is still valid → **Increase in integration scale**
- **Digital signal processing** part more and more replaces analog one (250nm → 10 K gates/mm² ... 28 nm → 3900 K gates/mm²)
- **Design cost** is increased comparing to manufacture one
- Design **timeline** and number of prototype cycles (respins) are reduced
- For the majority of projects the minimum set of ASICs is to be developed in a one well verified process (LHC → IBM 130 nm, SLHC → TSMC 130&65 nm, FAIR → UMC 0.18 µm) → **Standardization**
ASIC development trends (2)

- ASIC adaptation for other projects as criterion of economic efficiency → **Universalization** For ex., CBM STS & MUCH should be served by the same ASIC, having changeable front-end (preamp-shaper)
- Functionality increase at a limited **power consumption** budget
- Increase in demand for a high technology (expensive) product. The accent at design is done at system (architectural) questions → **SOCs** (systems on a chip) dictate a **mixed-signal** character of design flow
- The demanded number of ASIC wafers is small and can't interest a manufacturer (10^6 channels at ~100 chs/chip and ~1000 chips/wafer → ~10 wafers only)
Design is based on the usage of constantly modernized:

1) Computer Aided Design (CAD) systems (Cadence, Mentor Graphics, Synopsys, Agilent),
2) technological libraries or Design Kits (elements, standard digital and IP blocks), including
3) design rules of manufacturer, the quantity of which quickly grows for advanced technologies (> 2000 for 22 nm)

- Necessity of a fast and actually continuous retraining of experts
- Close integration of the design centers for both chip and system (hardware) level
Technology choice for FAIR

- Use technologies more and more advanced (with life time till 2020), but well characterized for design tools and having a reasonable cost → **UMC MMRF CMOS 0.18 μm** – main technology for FAIR (choice of 2005)

- Extremely compressed timeline for each cycle of custom design (4-6 months) and the presence of the necessary updated CAD tools at all levels of design

- Skilled staff of preferably **young engineers** (till 2020)

- Start-to-finish (system level) design is necessary: Structural and behavioral modeling → Design of IP blocks at transistor level and that of systems at high-level language → Layout → Verification (ERC, DRC, LVS, PE, PS) → GDSII
Radiation environment is not friendly

Radiation levels in Atlas: Charged particles, full view
Trends for radiation-hardened ICs

• Improvement of radiation hardness against total dose effects for new commercial CMOS processes. At the same time there is a wide spread of parameters among various manufacturers and no guarantee of long-term stability.

• Radiation-hardness processes lag behind commercial ones for 5-7 years (more than three generations according to Moore).

• Radiation hardening of modern ASICs is provided by a wider usage of commercial and a refinement of different methods and means, used at early design stages (rad-hard by design).

Trends for rad-hardened ICs (2)

- Rad-hard technologies are **not** economically efficient. For them there exists only a small volume of orders.

- Designer experience allows to carry out only a correct **choice** of the manufacturer, who can provide specific target requirements.

- Active **investigation** of radiation **effects** for new bulk CMOS technologies and their **compiling** into the standard of design rules and CAD tools (Calibre, Assura, QRC, etc.) both at element and behavioral levels.
Short summary on rad-hard ASICs

• A number of rad-hard applications will demand the design of rad-hard components and their manufacture in a radiation hardened technology to meet rigid requirements. The part of such ASICs will be decreased each year.

• Continuous improvement of very complex rad-hard systems will critically depend on the introduction of commercialized microelectronic innovations in these systems.

• Raising the limiting complexity of these systems to the level, reached in commercial technologies, will demand a shift of many projects in the direction of creating radiation-tolerant components, using traditional commercial technologies, applying the methods of maintaining an acceptable radiation hardness.
Actual task – analytical comparison of technologies by the radiation hardness:

1) Industrial (commercial) CMOS technology with use of methods “rad-hard-by-design”

2) Rad-hardened technology, according to the Moore law, lags more than 3 generations behind the commercial CMOS one

Thus, the practical dilemma is:

What is better

either a rad-hard 350 nm process
(for example, silicon-on-isolator)
or
a bulk CMOS 130 (90) nm process?
Traditional methods for radiation hardening

- Circuital (reservation, redundancy, coding, adaptive biasing and & so on)

- Layout (guard rings, ring transistors, and so on)

- Technological (low volume CMOS, SOI, trench isolation, & so on). The required rad-hardness level is provided by a semiconductor structure choice and use of the special technological processes
Rad-hard by design concept

- **Refinement** of traditional non-rad hard libraries for CAD
- **Elaboration** of additional **design rules**, improving rad-hardness at the following 3 levels of design:
  1) Transistor level
  2) Level of cells, gates and IP blocks
  3) System level
- Creation of calibrated **test structures** and expansion of the scaled element libraries
- Monitoring and statistical analysis of the ASIC rad-hard **stability**, provided at manufacture
- Rad-hard tests of chips at both **passive and active** work **modes**
Backgrounds for an ASIC design center in MEPhI

1) Now MEPhI is the **National Research Nuclear University – NRNU MEPhI**

2) The **experience** on chip design in joint research projects with leading RF enterprises

3) Full membership (A47530) in **Europractice** since 2003

4) Participation in a number of **International** physical experiments (incl. ATLAS, ALICE in CERN and CBM at FAIR)

5) Starting from 1996 MEPhI has direct **licensed agreements** with Cadence, Mentor Graphics, Synopsys, Agilent
offers at a reasonable price:

- licensed CADs of world leaders
- access to design rules and technological libraries (design kits) for a number of nanometer and submicron (40 nm ... 0.8 µm) processes, including SiGe, SOI, A₃B₅
- access to microsystem and MEMS technologies

provides an inexpensive (360...7900 Euro/sq.mm) prototyping of ASICs via advanced processes (down to 40 nm CMOS) using the so called multiproject approach, when the wafer cost is shared among projects of many customers

since 2013 Europractice provides discounted pricing for Russia as well as EU
# ASIC Multi-Project Wafer Schedule 2015

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<th>January</th>
<th>February</th>
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<td>Tue</td>
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![Calendar Image](http://www.europractice-ic.com/docs/EP_wall_calendar_2015.pdf)
Number of ASIC projects, manufactured via Europractice *

Total: 544 projects (6 from RF)

### Number of Russian ASIC projects, manufactured via Europractice *

<table>
<thead>
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<th>Russia</th>
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<tr>
<td><strong>Budker Institute of Nuclear Physics</strong></td>
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<tr>
<td><strong>IPMCE</strong></td>
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<td><strong>JSC “NTLAB”</strong></td>
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<td><strong>Moscow Institute of Electronic Technology</strong></td>
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<td><strong>Moscow Institute of Physics and Technology</strong></td>
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<td><strong>Moscow Engineering Physics Institute</strong></td>
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<tr>
<td><strong>N.I. Lobachevsky State Univ</strong></td>
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<tr>
<td><strong>SRIET-SMS CJSC</strong></td>
<td>6</td>
</tr>
<tr>
<td><strong>University St Petersburg</strong></td>
<td>5</td>
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<tr>
<td><strong>Vladimir State University</strong></td>
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* Europractice annual report 2014, C.38  
The infrastructure is financed since 2013 by a grant given by the Russian Federation Government based on resolution №220. The head of Lab is V. Samsonov

- Development Russian design center of Application Specific Integrated Circuits with technological nodes of 40-180 nm.
- Design of ASICs for well recognized International and Russian experiments (for ex. CBM, NIKA)
- Development of competence center on chip design. Organizing topical Conferences, Workshops, Master classes.
- Research of new project solutions, test prototyping and small volume production
Infrastructure of the ASIC design center

- distributed interdepartmental 1 Gb/s local Intranet
- clusters of network SUN and Linux workstations in a number of departments
- licensed microelectronics tools for computer aided design – Cadence, Mentor Graphics, Synopsys, Agilent
- computer classes for core students
- technological libraries (Design Kits) starting from 40 nm
Organization of All-Russia Workshops

• AMS Methodology Kit Workshop
  **22-24 September 2009**

• II Workshop on mixed-signal IC design
  **10 - 14 October 2011**

• Youth school on CAD tools for mixed-signal IC design for physical instrumentation
  **11 - 14 September 2012**

• IV Methodology Workshop on CAD tools for mixed-signal IC design for physical instrumentation
  **29-31 October 2013**

• V Methodology Workshop on CAD tools for mixed-signal IC design for physical instrumentation
  **8-11 December 2014**
IV Всероссийский научно-методический семинар по средствам проектирования интегральных микросхем для аппаратуры физического эксперимента

29-31 октября 2013 года

Приглашаем вас принять участие в работе семинара.


Цель семинара - познакомить участников с методикой автоматизированного проектирования смешанных (аналого-цифровых) интегральных микросхем, развиваемой компанией Cadence, и провести практические мастер-классы с целью популяризации микроэлектронных САПР для предприятий высокотехнологичного сектора экономики РФ. Приоритет будет отдан предприятиям ГК "Росатом", осуществляющим крупные проекты, такие как на международных ускорителях ФАИР (г. Дармштадт, Германия) и НИКА (г. Дубна).

Важная часть семинара - тематические лекции приглашенных известных в мире ученых из CERN (Женева), GSI (Дармштадт), AGH (Краков), отражающие последние мировые достижения в области реализации и внедрения сложнофункциональных интегральных микросхем для аппаратуры физического эксперимента.

Более подробная информация представлена на сайте: cad.mephi.ru.
ASIC projects

- 128-channel prototype ASIC for data-driven read-out of CBM STS
  
  0.18 um CMOS UMC (Taiwan), consumption 2 mW/ch., shaping time 100 ns, structure 128→16/ Chip contains preamplifier, shaper (filter), comparators, cross-point switch, peak detectors, 9-bit ADC and so on

- Smart sensor readout ASIC (Rosatom)
  
  0.35 μm SiGe BiCMOS AMS (Austria), temperature range -55...+80 °C, consumption 3 mW. Chip contains instrumentation amplifier, 14-bit ADC, two 14-bit DAC, references, electronic thermometer and so on

- 32-channel ASIC for “Nucleon” project (Roscosmos)
  
  0.35 μm CMOS AMIS/OnSemi (Belgium), dynamic range 100 pC/D, consumption 2 mW/ch., multiplexed (serial) output

- IP blocks for system on chip, controlling a new aircraft engine (Ministry of Education and Science)
  
  0.18 um CMOS UMC (Taiwan), consumption 10 mW/ch., 9-bit ADC
SOME DETAILS OF ASIC PROJECTS

32-channel ASIC for Nucleon project of ROSCOSMOS

128-channel prototype ASIC for CBM STS
Tests for total dose effects

(E=8 MeV; F=10^{11} e/cm^2 s; D=0.1; 1; 3 Mrad)

1) Threshold voltage shift (~100 mV);
2) Leakage currents  --- standard (strip-like) nMOS;
   --- ring transistors
Phase I: Design of analog and mixed-signal ASICs

Phase II: Prototyping and test technique development

Phase III: First tests and prototype characterization

Phase IV: Qualification of ASICs

Phase V: Preparation for a batch production and testing automation
1. Route «bottom-to-top» (traditional)

**Feature:** the possibility to perform a mixed-signal simulation for analysis of blocks interaction appears only after the all separate blocks being ready.
Feature: the usage of mixed-signal simulations at early stage. Due to system synthesis at structure level, it becomes possible to develop fastly the block descriptions at behavioral level – RTL-Verilog, Verilog-A и Verilog-AMS. The same level of abstraction is available with VHDL.
Modern ASICs, as a rule, are **mixed-signal** chips. They surely include both analog and digital parts.

Analog part is designed as a custom block, whereas the digital one is described by VHDL or Verilog and then synthesized as a semicustom block, based on standard digital libraries.

Now a system simulation at element (transistor) level requires unacceptably a lot of time.

Usage of high description languages and software tools for **hierarchy** design allows to perform simulation with **different abstractions** level of blocks.
Traditional design routes

**Analog Circuit Design flow**
- **System Modeling**
  - Verilog-A, ideal blocks
- **Schematic Capture + Simulation**
  - Transistor level design & simulation
- **Layout**
  - Full custom layout, matching
- **Physical Verification**
  - DRC & LVS check
- **Post-simulation**
  - Parasitic extraction and post-layout simulation
- Cadence schematic editor + Spectre
- Cadence layout editor
- Mentor Calibre
- Cadence Spectre

**Digital Circuit Design flow**
- **HDL code entry**
  - Verilog / VHDL
- **Behavioral simulation**
  - Writing testbench to verify functional & timing
- **Logic synthesis**
  - Behavioral code to structural verilog code bound to library
- **Physical synthesis**
  - Place and route
- **Post-simulation**
  - Parasitic extraction and post-layout simulation
- Model sim, Xilinx ISE simulator
- Model sim, Xilinx ISE simulator
- Synopsys Design Compiler
- Cadence SOC encounter
- Cadence
Usage of high description languages and software tools for **hierarchy** design allows to perform simulation with **different abstraction** level of separate blocks.

**Design aspects, taking into account the requirements on radiation hardness**
• Verilog description of whole ASIC
• Analog blocks are described as digital modules without functions, but with interface part
• Project compilation in gate level verilog
• For debugging it is necessary to have layout views of both standard library elements and analog blocks in format LEF (library exchange format)
• Few next stages are made in SoC Encounter, namely: placement of analog blocks, placement of digital part, routing of power supply buses, routing of signal wires
Smart pressure sensor readout ASIC

Customer – Rosatom

Design duration – 8 months of 2010

Chip planning in SoC Encounter (Cadence)
**Instrumentation amplifier**

<table>
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</tr>
<tr>
<td>Unity gain frequency</td>
<td>2 MHz</td>
</tr>
<tr>
<td>Phase margin</td>
<td>70 degree</td>
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<tr>
<td>Consumption current</td>
<td>100 µA</td>
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<tr>
<td>RMS noise</td>
<td>20 nV/Hz$^{1/2}$</td>
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<td>Temperature range</td>
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<tr>
<td>Input current</td>
<td>5 nA</td>
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<tr>
<td>Offset voltage</td>
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Prototyped via Europractice in 2010:
SiGe 0.35 µm BiCMOS of AMS
Test bench: circuit and board
14-bit DAC

<table>
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<th>DAC1</th>
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<tr>
<td>Number of bits</td>
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<tr>
<td>Output range</td>
<td>3.9 V</td>
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<tr>
<td>Differential nonlinearity</td>
<td>1 LSB</td>
</tr>
<tr>
<td>Integral nonlinearity</td>
<td>2 LSB</td>
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<tr>
<td>Consumption current</td>
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</table>

![Graph showing the output voltage over time](image)
 Library of reusable IP blocks

Parameters:
- Consumption
- Speed
- Dynamic range

Tasks:
- Track finding
- Calorimetry
- Charge detection
- Time of flight

Derandomizer
Slow Control
HDR readout
Data-driven readout
Analog readout chain

IP blocks
- Comparators
- Driver
- CSA
- Opamp
- PD
- T/H
- S/H
- Cross-point switch
- Arbitration Logic
- MUX
- Control Logic

How to build an hierarchy?
ASIC for Nucleon project*

- Large dynamic range (100pC), consumption 2mW/ch, 32 chs.
- Prototyped in 2005-2009 and reproduced in 2012
- AMIS 0.35 um CMOS process
- 6 respins:
  1) Analog, 16 CSAs (включен в отчет Europractice 2005г.) Feb 2005
  2) Mixed-signal, 4+2(тест.) CSA+SH+T&H+MUX+Driver Sept 2006
  3) Mixed-signal, 4+2(тест.) CSA+SH+T&H+MUX+Driver Feb 2007
  4) Mixed-signal, 32+2 (тест.) CSA+SH+T&H+MUX+Driver Apr 2007
  5) Mixed-signal, 32+2 (тест.) (включен в отчет Europractice 2009г.) CSA+SH+T&H+MUX+Driver Sept 2009
  6) Мелкосерийное производство. Mixed-signal, 32+2 (тест.) CSA+SH+T&H+MUX+Driver Apr 2012
- Late 2014 ASIC has been launched from Baikonur to the Space

* ROSCOSMOS project (to be presented by A. Voronin)
ASIC Structure

- **in_dummy0**: Connected to `in_0`, `in_1`, `in_2`, `in_3`
- **Shift reg**: Connected to `in_dummy0`, `in_0`, `in_1`, `in_2`, `in_3`
- **MUX**: Connected to `in_dummy0`, `in_0`, `in_1`, `in_2`, `in_3`
- **Test channel 0**: Connected to `in_dummy0`, `in_0`, `in_1`, `in_2`, `in_3`
- **Channel 1**: Connected to `in_dummy0`, `in_0`, `in_1`, `in_2`, `in_3`
- **Channel 2**: Connected to `in_dummy0`, `in_0`, `in_1`, `in_2`, `in_3`
- **Channel 3**: Connected to `in_dummy0`, `in_0`, `in_1`, `in_2`, `in_3`
- **Channel 4**: Connected to `in_dummy0`, `in_0`, `in_1`, `in_2`, `in_3`
- **Test channel 1**: Connected to `in_dummy0`, `in_0`, `in_1`, `in_2`, `in_3`
- **Calibr.**: Connected to `in_dummy0`, `in_0`, `in_1`, `in_2`, `in_3`
- **Bias block**: Connected to `in_dummy0`, `in_0`, `in_1`, `in_2`, `in_3`
- **Conversion U --> I**: Connected to `in_dummy0`, `in_0`, `in_1`, `in_2`, `in_3`
- **out dummy0**: Connected to `in_dummy0`, `in_0`, `in_1`, `in_2`, `in_3`
- **out 0**: Connected to `in_dummy0`, `in_0`, `in_1`, `in_2`, `in_3`
- **out 1**: Connected to `in_dummy0`, `in_0`, `in_1`, `in_2`, `in_3`
- **out 2**: Connected to `in_dummy0`, `in_0`, `in_1`, `in_2`, `in_3`
- **out 3**: Connected to `in_dummy0`, `in_0`, `in_1`, `in_2`, `in_3`
- **out dummy1**: Connected to `in_dummy0`, `in_0`, `in_1`, `in_2`, `in_3`
- **Shift_out_b**: Connected to `in_dummy0`, `in_0`, `in_1`, `in_2`, `in_3`

**Analog Storage + Analog Multiplex**
- Prebias
- Shaper
- MUX
- ADC
- Storage (TE/TEPD)
- INL
- INH
- OUTL
- OUTH

**Bufferless to deadtime**
- **Long readout time**
Differential Current drivers

Digital part

References
Scope diagrams

CSA structure

CSA/shaper response

CSA tail adjustment

Output current driver

Typical waveforms
Some relevant references

1. International technology roadmap for semiconductors, 2009 Executive summary

   in Particle Physics, Bariloche, Argentina, 2010 www-physic.lbl.gov/~spieler

   international meeting on Front End Electronics for High Energy, Nuclear, Medical, and Space


5. R. Lacoe, Improving Integrated Circuit Performance Through the Application of

6. K. Roy, B. Jung, A. Raghunathan, Integrated systems in the more-than-Moore Era:
   Designing lowcost energy efficient systems using heterogeneous components/
   23rd International Conference on VLSI Design, 2010
Some relevant references (II)

7. Marchioro A Microelectronics for Instrumentation in Physics 2012 Proc. All-Russian Workshop on Electronics at MEPhI
8. Snoeys W Microelectronics for Instrumentation in Physics 2013 Proc. All-Russian Workshop on Electronics at MEPhI
Conclusions

The future of particle physics and astrophysics instrumentation is tightly bound with a wide usage of **ASiCs** due to the new challenge in integration scale.

The solution of **system** (architectural, structural) problems will demand substantially higher efforts. Actually there is the question of creating not separate components, but whole systems on chip (**SoC**).

Almost all new chips have a **mixed-signal character**.

Nowadays the design is based on microelectronic **CADs** and the adapted **Design Kits** of the chosen manufacturer.

**Reduction of timelines** for design, extension of reusable IP block libraries, new level of **system tests** for readout electronics – all of that requires the usage of advanced CAD in distributed fast networks of powerful computing clusters.
Conclusions (2)

The “Rad-hard by design” approach for commercial CMOS technology is considered to be the best way of providing an acceptable rad-hardness by circuitual and layout techniques.

For rad-hardness and temperature stability of the chips it is important to refine the existing libraries and design routes.

Long term planning becomes an extremely important factor, especially taking into account the “life time” of both the chosen technology and the design staff.

The necessity of a wider collaboration between the design centers and research institutions, sharing the process of preparing human resources and the cost of using expensive CAD.
Thanks for your attention

ICPPA-2015, 5-10 Oct 2015, Moscow
Back ups

- Technological level in Russia
The Federal Target Program "Development of Electronic Component Basis and Radioelectronics" for 2008 - 2015

Approved by the Government on November, 26th, 2007, decree N 809

2 main target indicators:

- The technological level of modern electronic component basis is estimated, basing on the one of microelectronic products, mastered in manufacture

  - 2008 → 0.18 µm
  - 2011 → 0.09 µm
  - 2015 → 0.045 µm

- There should be created 64 chip design centers in Russia

Important current tasks for Russia:

- A new Federal program on developing a chip design center network, comprising up to 150 centers, has been approved
- Creation of an advanced national photomask center