ASIC DESIGN FOR PARTICLE PHYSICS AND ASTROPHYSICS

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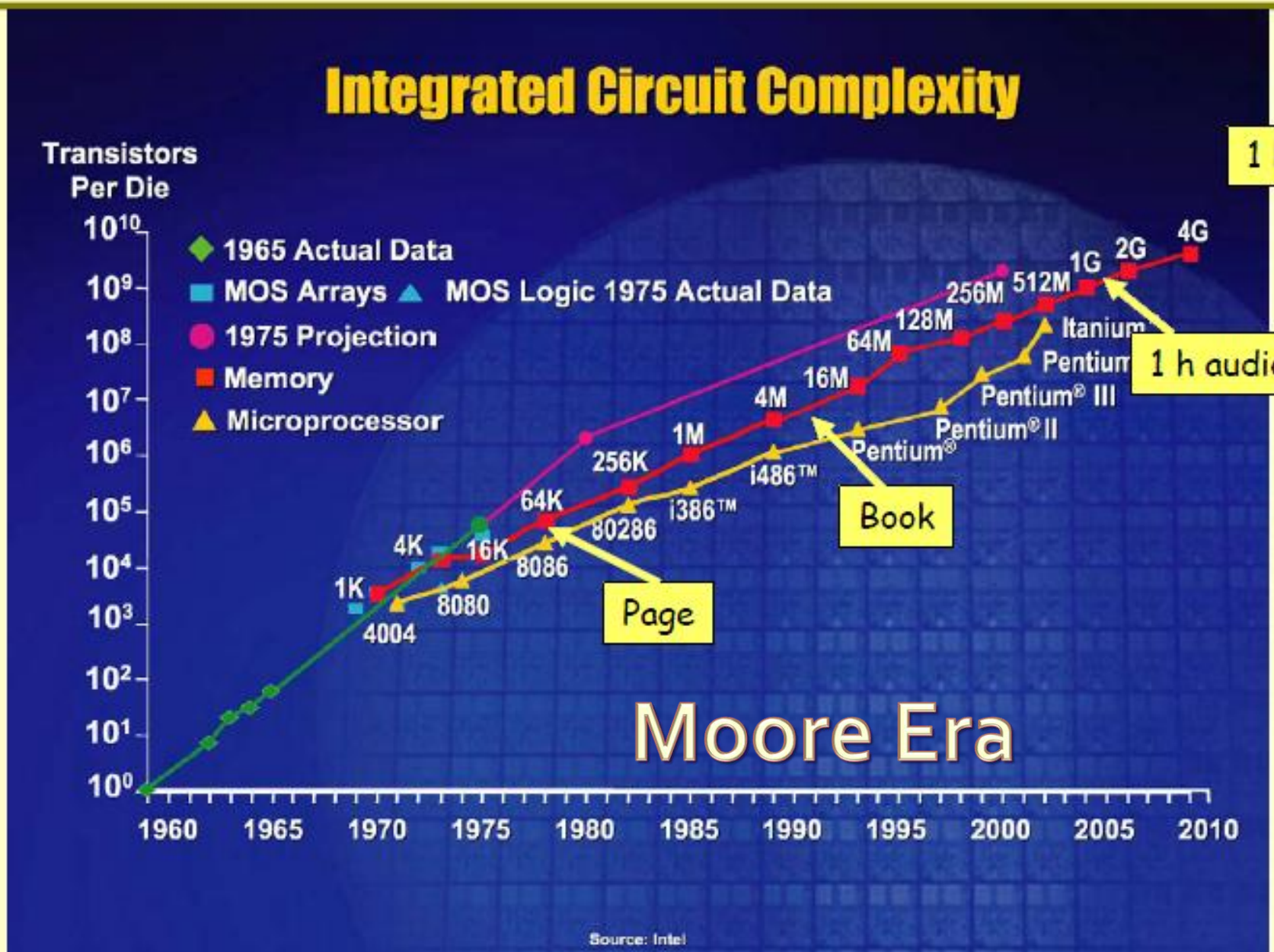
Abstract

- ASICs are one of the **key** complex **technologies** available to detector designers
- ASICs are essential for **integration scale**, **low power dissipation**, **high speed capability**, **radiation tolerance**
- For future experiments in the intensity, cosmic, and energy frontiers ASICs should provide new level of functionality at a **new set of constraints and trade-offs**, like low-noise high-dynamic range amplification and pulse shaping, high-speed waveform sampling, low power digitization, fast digital data processing, serialization and data transmission
- All chips should allow minute almost 3D assemblies
- The talk presents overview of the state of the art and **trends** in nowadays chip design, basing partially our ASIC lab experience.

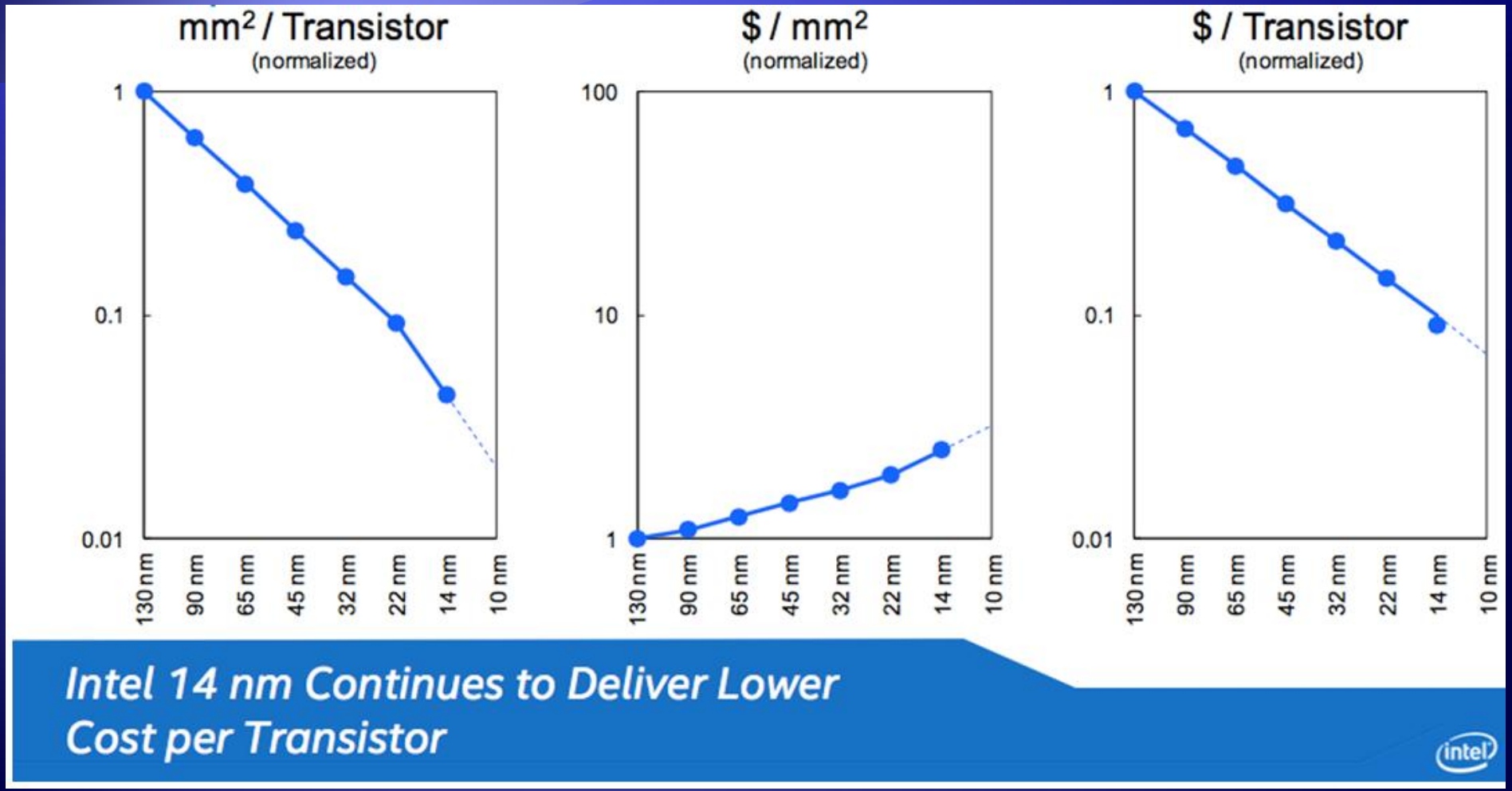
Plan

- Trends in integrated circuit development
- Experience in establishing the ASIC design center
- Design center infrastructure
- Chip prototyping
- Design route and its main stages
- Example projects
- Conclusions

Trend: $N(x) = A * \exp(t/\tau)$ $\tau \sim 18$ months



Cost per transistor

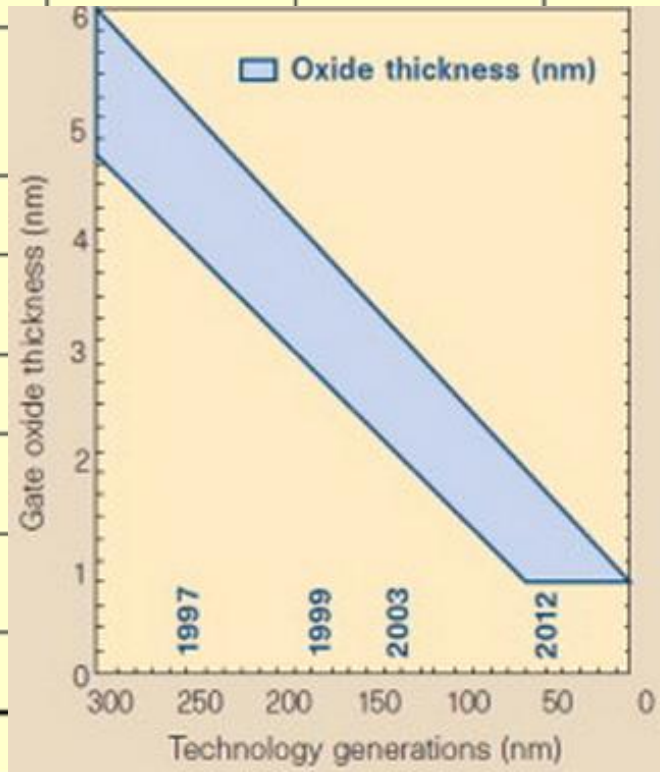


Up-to-date world-wide technologies

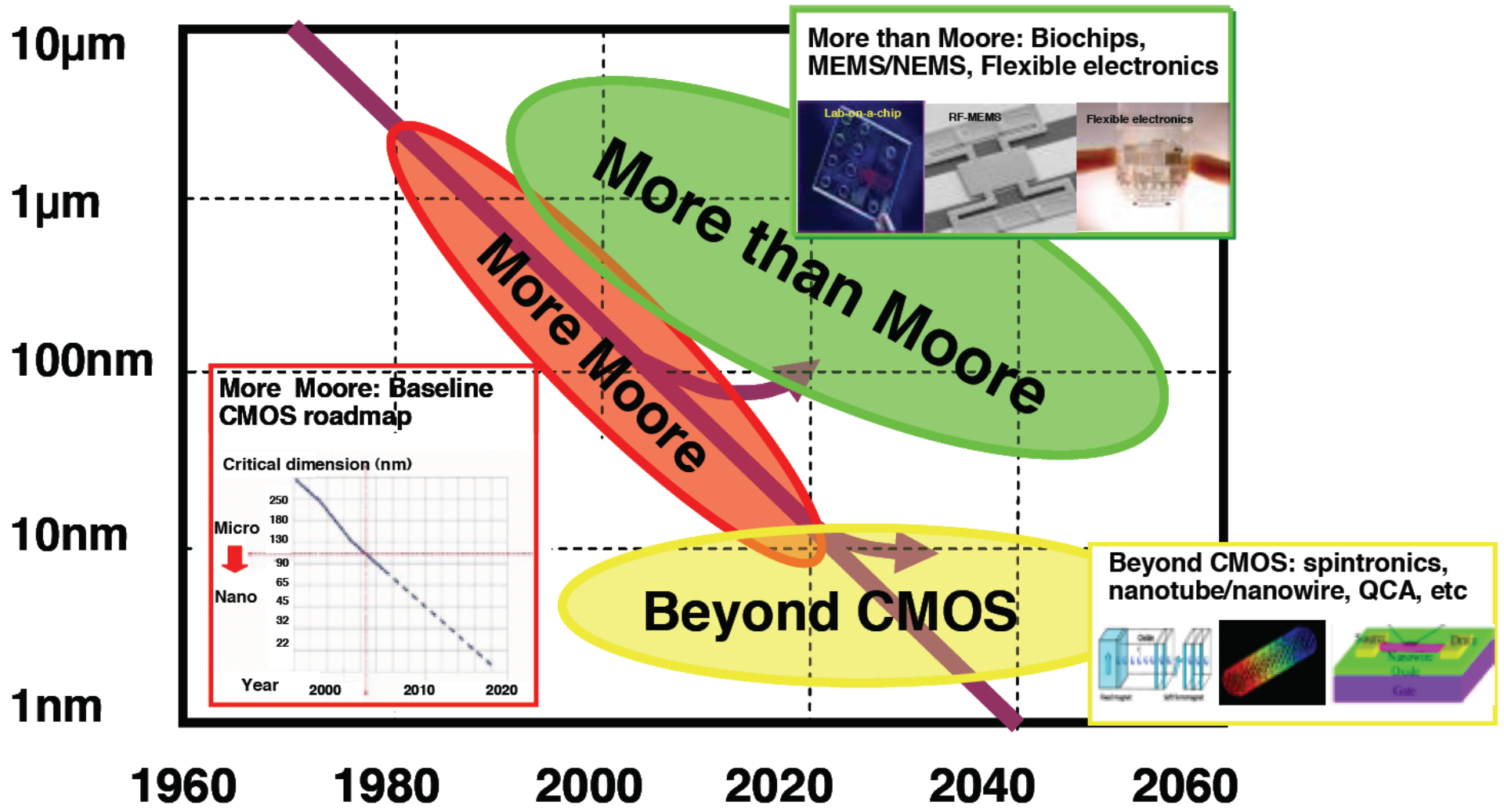
ITRS Roadmap

	2004	2007	2010	2013	2016
Technology Node [nm]	90	65	45	32	22
Transistor count [Mtr]			1500	3092	6184
Transistor Density [Mtr/cm2]	77	154			
Chip Size	140				
Clock freq [GHz]	3				
Vdd	1.2	1.1			
DRAM half pitch	90	65			
Signal IO Pads	512	1024			
Power Pads	1024				

International Technology Roadmap for Semiconductors



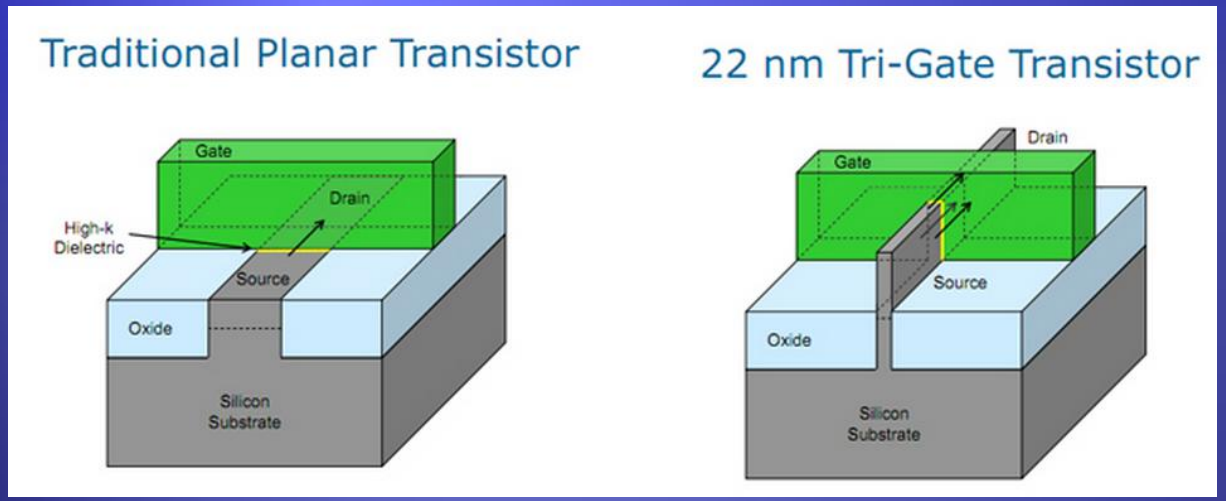
Technology variety

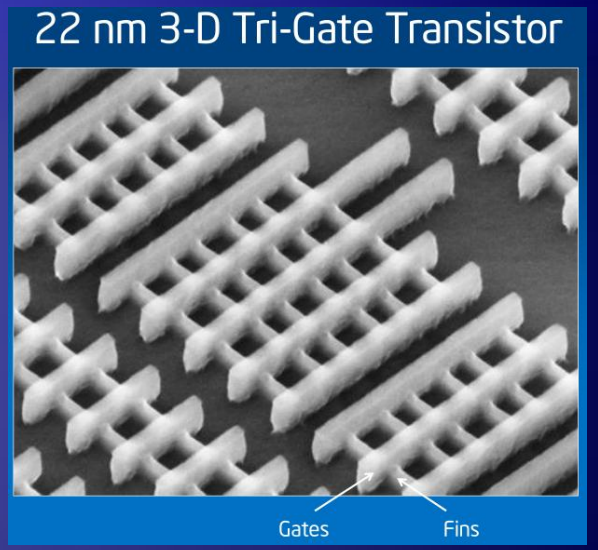


K.Roy, B.Jung, A.Raghunathan, Integrated systems in the more-than-Moore Era: Designing low-cost energy efficient systems using heterogeneous components/ 23rd International Conference on VLSI Design, 2010

What is after More Moore?

CMOS technology has followed Moore's Law for 50 years, shrinking devices and interconnect to smaller and **smaller dimensions**, with many technological tricks and challenges to achieve this in the transistors, the **lithography** and the **metallization**



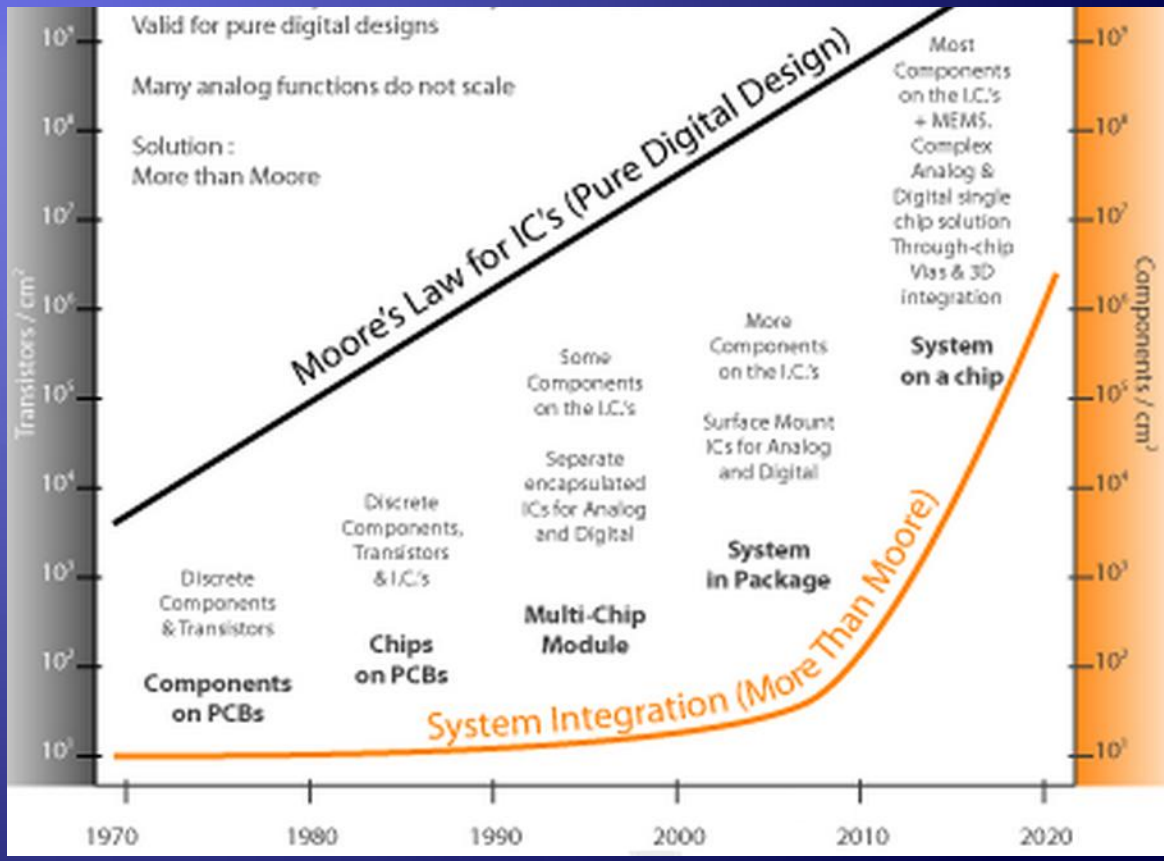


In 2011 Intel made a significant innovation of the first 22nm 3-D **tri-gate** silicon transistors. Instead of a thinner dielectric, transistors were redesigned with wider dielectric layers that surround a **fin shape**. This improves the control of electric field, reduce current densities and leakage, and diminish process variations

More than Moore

Functional **diversification***:
Incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law“, but provide **additional value in different ways**

The approach allows for the non-digital functionalities to migrate from the system board-level into the package (SiP) or onto the chip (SoC)

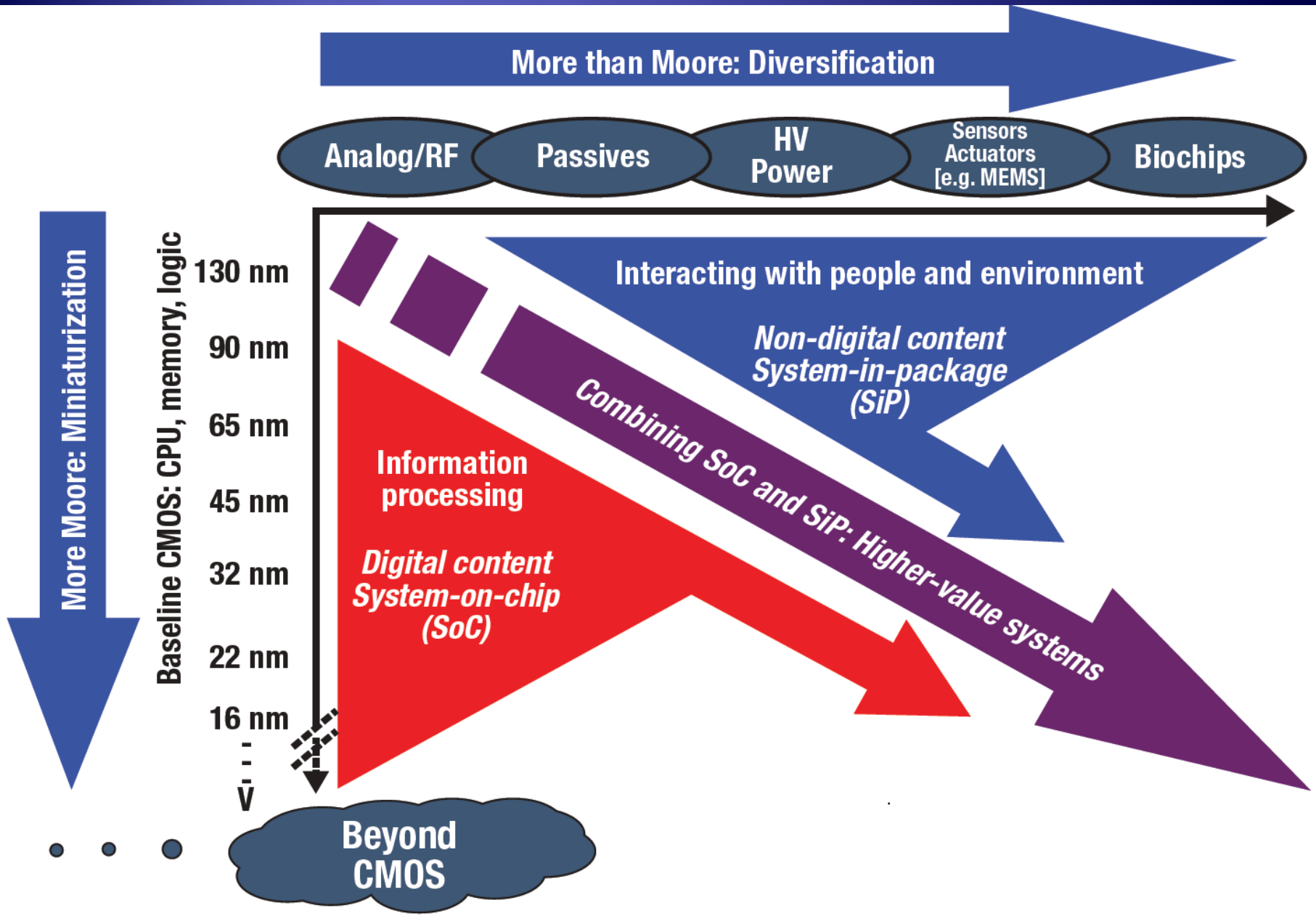


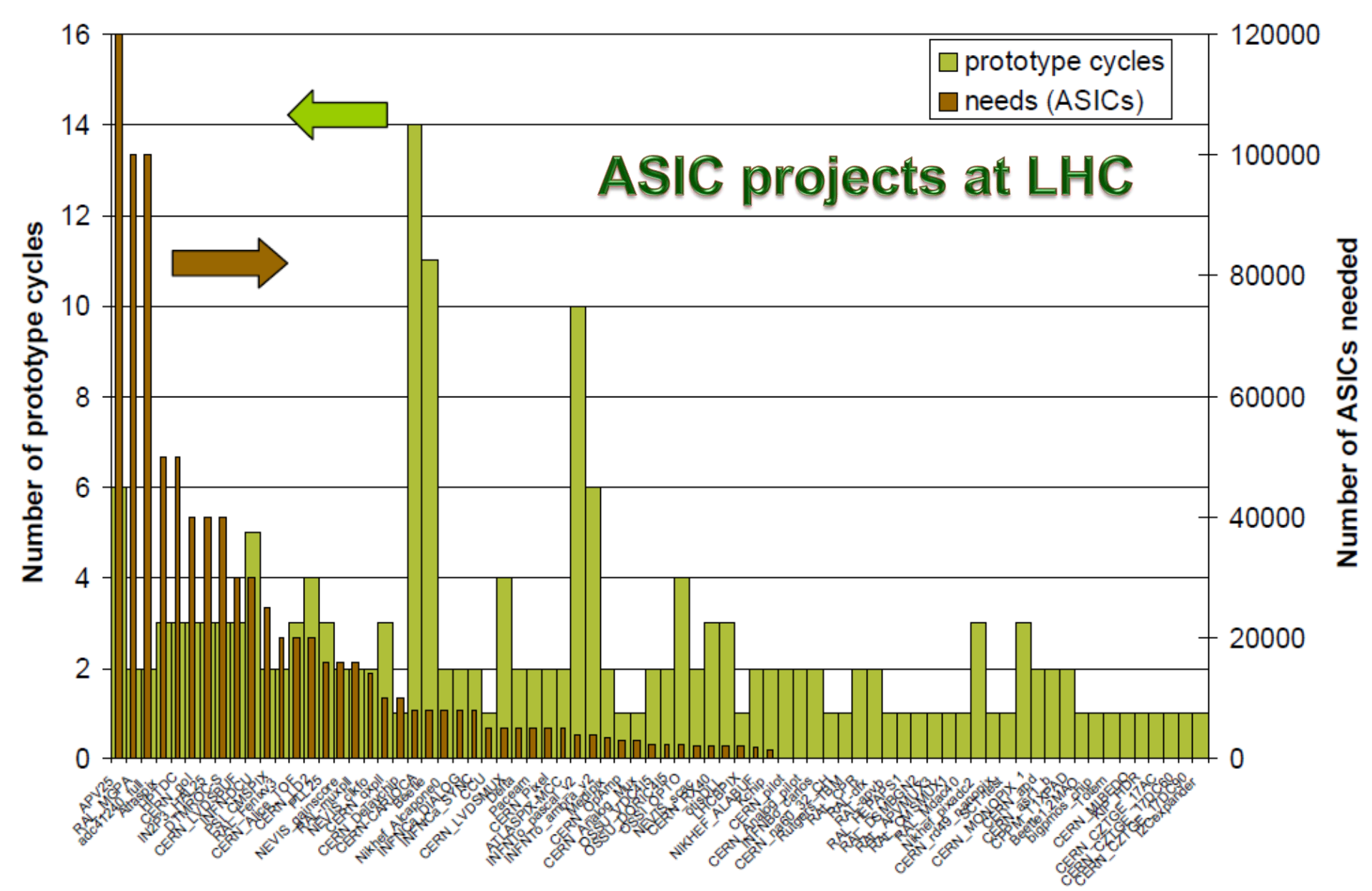
* “More-than-Moore” White Paper, http://www.itrs.net/ITRS%201999-2014%20Mtgs,%20Presentations%20&%20Links/2010ITRS/IRC-ITRS-MtM-v2%203.pdf

More than Moore

- FinFet
- Fully Depleted SOI
- Through-silicon via
- Wafer-to-wafer stacking
- Truly 3D monolithic CMOS
- New materials (III-IV, Ge, GaN, SiC, etc.)
- New phenomena: non kT/q controlled thresholds slopes
- …

More than Moore





Each strip corresponds to a separate ASIC project

No correlation between the number of prototype cycles and the number of ASICs needed

A. Marchioro, "Can HEP Afford Private MPW Runs in the Future?", Proc. 5th international meeting on Front End Electronics for High Energy, Nuclear, Medical, and Space Applications, Snowmass Village, Colorado, June 2003

CMS

ASIC development trends

- The increasing quantity of elements at a simultaneous increase in their complexity and density. Moore law is still valid → **Increase in integration scale**
- **Digital signal processing** part more and more replaces analog one (250nm → 10 Kgates/mm^2 … 28 nm → 3900 Kgates/mm^2)
- **Design cost** is increased comparing to manufacture one
- Design **timeline** and number of prototype cycles (respins) are reduced
- For the majority of projects the minimum set of ASICs is to be developed in a one well verified process (LHC → IBM 130 nm, SLHC → TSMC 130&65 nm, FAIR → UMC 0.18 μm) → **Standardization**

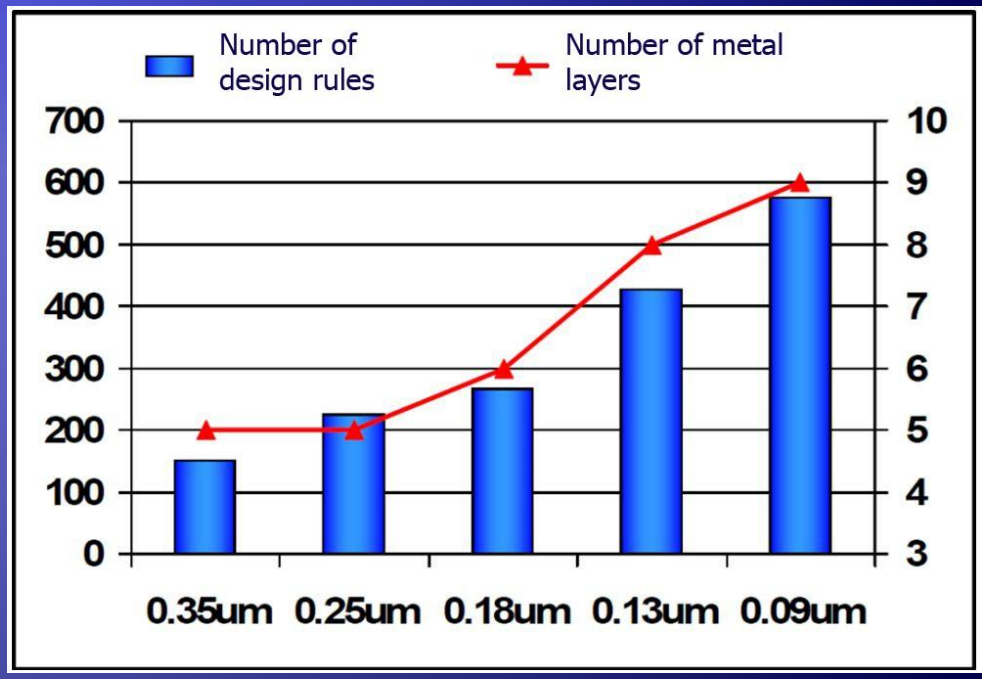
ASIC development trends (2)

- ASIC adaptation for other projects as criterion of economic efficiency → **Universalization** For ex., CBM STS & MUCH should be served by the same ASIC, having changeable front-end (preamp-shaper)
- Functionality increase at a limited **power consumption** budget
- Increase in demand for a high technology (expensive) product. The accent at design is done at system (architectural) questions → **SOCs** (systems on a chip) dictate a **mixed-signal** character of design flow
- The demanded number of ASIC wafers is small and can't interest a manufacturer (**10^6 channels** at ~100 chs/chip and ~1000 chips/wafer→ ~**10 wafers** only)

ASIC development trends (3)

- Design is based on the usage of constantly modernized:

1) Computer Aided Design (**CAD**) systems (Cadence, Mentor Graphics, Synopsys, Agilent),
2) technological libraries or **Design Kits** (elements, standard digital and IP blocks), including
3) design **rules** of manufacturer, the quantity of which quickly grows for advanced technologies (> 2000 for 22 nm)

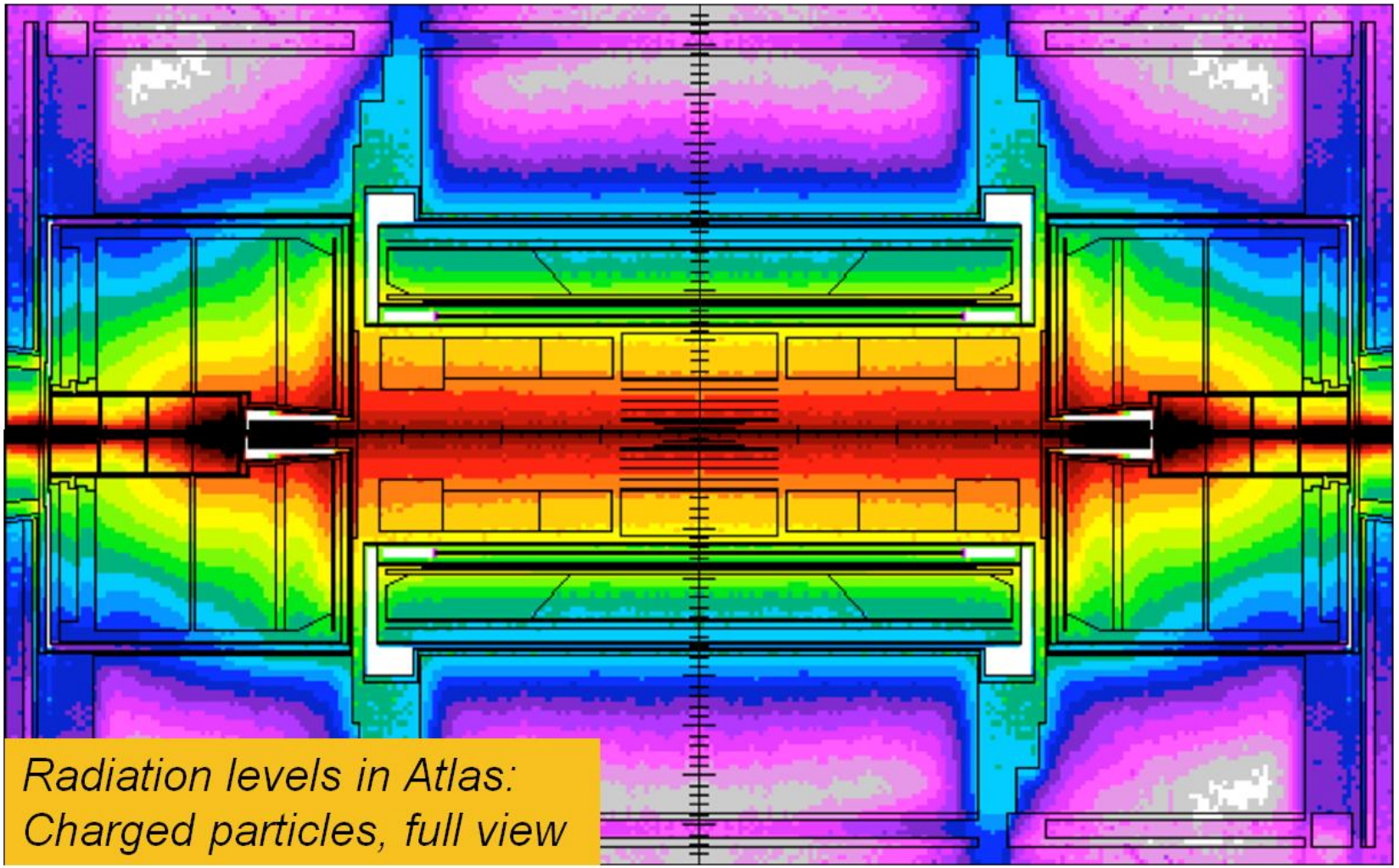


- Necessity of a fast and actually continuous **retraining** of experts
- Close **integration** of the design centers for both chip and system (hardware) level

Technology choice for FAIR

- Use technologies more and more advanced (with life time till 2020), but well characterized for design tools and having a reasonable cost → **UMC MMRF CMOS 0.18 µm** – main technology for FAIR (choice of 2005)
- Extremely compressed timeline for each cycle of custom design (4-6 months) and the presence of the necessary updated CAD tools at all levels of design
- Skilled staff of preferably **young engineers** (till 2020)
- Start-to-finish (system level) design is necessary: Structural and behavioral modeling → Design of IP blocks at transistor level and that of systems at high-level language → Layout → Verification (ERC, DRC, LVS, PE, PS) → GDSII

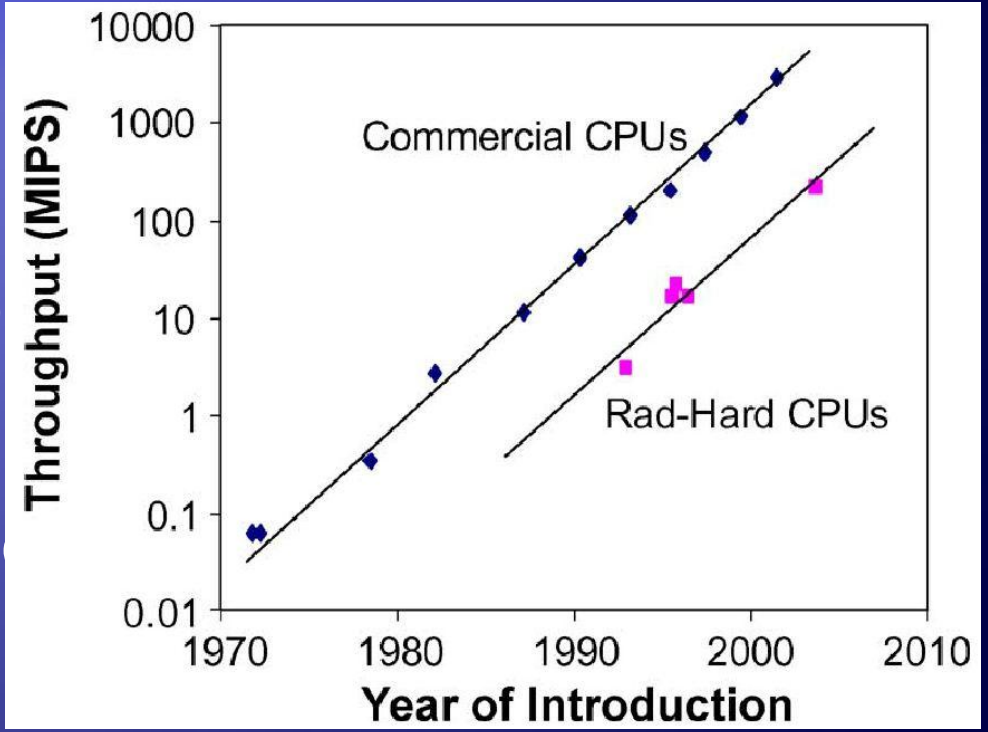
Radiation environment is not friendly



Radiation levels in Atlas:
Charged particles, full view

Trends for radiation-hardened ICs

- Improvement of radiation hardness against total dose effects for new **commercial CMOS** processes. At the same time there is a wide spread of parameters among various manufacturers and no guarantee of long-term stability
- Radiation-hardness processes **lag behind** commercial ones for 5-7 years (more than three generations according to Moore)
- Radiation hardening of modern ASICs is provided by a wider usage of commercial and a refinement of different methods and means, used at early design stages (**rad-hard by design**)



R. Lacoe, Improving Integrated Circuit Performance Through the Application of Hardness-by-Design Methodology IEEE Transaction on Nuclear science, v. 55, N4, 2008, p.1903-1925

Trends for rad-hardened ICs (2)

- Rad-hard technologies are **not** economically efficient. For them there exists only a small volume of orders
- Designer experience allows to carry out only a correct **choice** of the manufacturer, who can provide specific target requirements
- Active **investigation** of radiation **effects** for new bulk CMOS technologies and their **compiling** into the standard of design rules and CAD tools (Calibre, Assura, QRC, etc.) both at element and behavioral levels

Short summary on rad-hard ASICs

- A number of rad-hard applications will demand the design of rad-hard components and their manufacture in a **radiation hardened technology** to meet rigid requirements. The part of such ASICs will be decreased each year
- Continuous improvement of very complex rad-hard systems will critically depend on the introduction of commercialized microelectronic innovations in these systems
- Raising the limiting complexity of these systems to the level, reached in commercial technologies, will demand a shift of many projects in the direction of creating **radiation-tolerant** components, using traditional commercial technologies, applying the methods of maintaining an acceptable radiation hardness

Actual task – analytical comparison of technologies by the radiation hardness:

- 1) Industrial (commercial) CMOS technology with use of methods “rad-hard-by-design”

- 2) Rad-hardened technology, according to the Moore law, lags more than 3 generations behind the commercial CMOS one

Thus, the practical dilemma is:

What is better

either a rad-hard 350 nm process
(for example, silicon-on-isolator)

or

a bulk CMOS 130 (90) nm process?

Traditional methods for radiation hardening

- Circuital (reservation, redundancy, coding, adaptive biasing and & so on)
- Layout (guard rings, ring transistors, and so on)
- Technological (low volume CMOS, SOI, trench isolation, & so on). The required rad-hardness level is provided by a semiconductor structure choice and use of the special technological processes

Rad-hard by design concept

- **Refinement** of traditional non- rad hard libraries for CAD
- **Elaboration** of additional **design rules**, improving rad-hardness at the following 3 levels of design:
  1) Transistor level
  2) Level of cells, gates and IP blocks
  3) System level
- Creation of calibrated **test structures** and expansion of the scaled element libraries
- Monitoring and statistical analysis of the ASIC rad-hard **stability**, provided at manufacture
- Rad-hard tests of chips at both **passive and active** work **modes**

Backgrounds for an ASIC design center in MEPhI

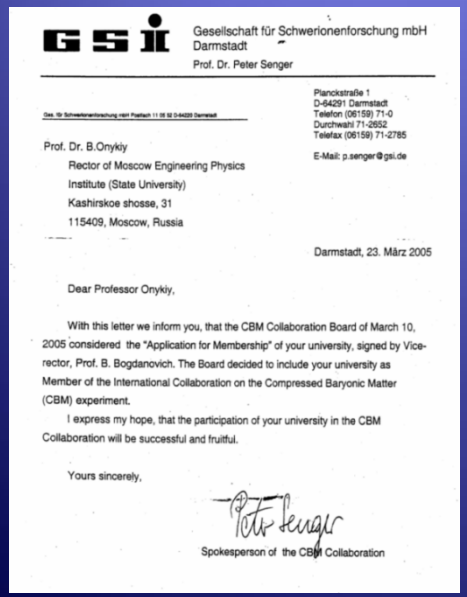
1) Now MEPhI is the **National Research Nuclear** University – NRNU MEPhI

2) The **experience** on chip design in joint research projects with leading RF enterprises

3) Full membership (A47530) in **Europractice** since 2003

4) Participation in a number of **International** physical experiments (incl. ATLAS, ALICE in CERN and CBM at FAIR)

5) Starting from 1996 MEPhI has direct **licensed agreements** with Cadence, Mentor Graphics, Synopsys, Agilent



GSI Gesellschaft für Schwerionenforschung mbH
Darmstadt
Prof. Dr. Peter Senger

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E-Mail: p.senger@gsi.de

Prof. Dr. B.Onykiy
Rector of Moscow Engineering Physics
Institute (State University)
Kashirskoe shosse, 31
115409, Moscow, Russia

Darmstadt, 23. März 2005

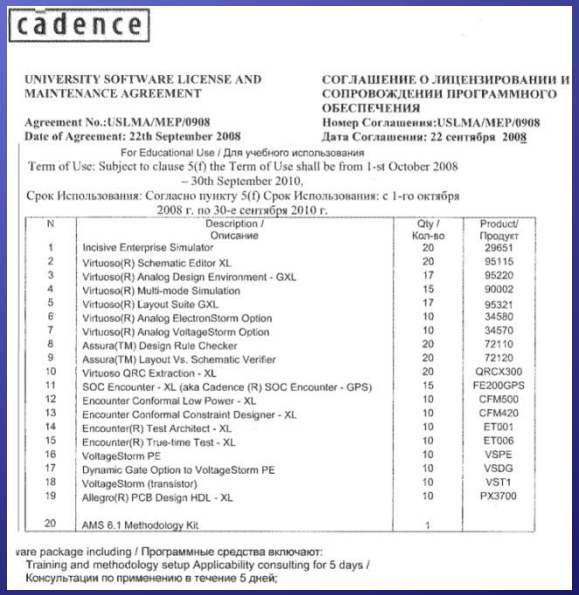
Dear Professor Onykiy,

With this letter we inform you, that the CBM Collaboration Board of March 10, 2005 considered the "Application for Membership" of your university, signed by Vice-rector, Prof. B. Bogdanovich. The Board decided to include your university as Member of the International Collaboration on the Compressed Baryonic Matter (CBM) experiment.

I express my hope, that the participation of your university in the CBM Collaboration will be successful and fruitful.

Yours sincerely,

Spokesperson of the CBM Collaboration



cadence

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СОГЛАШЕНИЕ О ЛИЦЕНЗИРОВАНИИ И СОПРОВОЖДЕНИИ ПРОГРАММНОГО ОБЕСПЕЧЕНИЯ

Agreement No.:USLMA/MEP/0908
Date of Agreement: 22th September 2008

Номер Соглашения:USLMA/MEP/0908
Дата Соглашения: 22 сентября 2008

For Educational Use / Для учебного использования

Term of Use: Subject to clause 5(f) the Term of Use shall be from 1-st October 2008 – 30th September 2010,

Срок Использования: Согласно пункту 5(f) Срок Использования: с 1-го октября 2008 г. по 30-е сентября 2010 г.

N	Description / Описание	Qty / Кол-во	Product/ Продукт
1	Incisive Enterprise Simulator	20	29651
2	Virtuoso(R) Schematic Editor XL	20	95115
3	Virtuoso(R) Analog Design Environment - GXL	17	95220
4	Virtuoso(R) Multi-mode Simulation	15	90002
5	Virtuoso(R) Layout Suite GXL	17	95321
6	Virtuoso(R) Analog ElectronStorm Option	10	34580
7	Virtuoso(R) Analog VoltageStorm Option	10	34570
8	Assura(TM) Design Rule Checker	20	72110
9	Assura(TM) Layout Vs. Schematic Verifier	20	72120
10	Virtuoso QRC Extraction - XL	20	QRCX300
11	SOC Encounter - XL (aka Cadence (R) SOC Encounter - GPS)	15	FE200GPS
12	Encounter Conformal Low Power - XL	10	CFM500
13	Encounter Conformal Constraint Designer - XL	10	CFM420
14	Encounter(R) Test Architect - XL	10	ET001
15	Encounter(R) True-time Test - XL	10	ET006
16	VoltageStorm PE	10	VSPE
17	Dynamic Gate Option to VoltageStorm PE	10	VSDG
18	VoltageStorm (transistor)	10	VST1
19	Allegro(R) PCB Design HDL - XL	10	PX3700
20	AMS 6.1 Methodology Kit	1	

ware package including / Программные средства включают:
Training and methodology setup Applicability consulting for 5 days /
Консультации по применению в течение 5 дней;

CLRC

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Date As Postmark

Dear Colleague

EUROPRACTICE FULL IC SERVICE SUBSCRIPTION

Thank you for the interest that you have shown in EUROPRACTICE.

Your **Full IC Service** Membership application has been approved and your EUROPRACTICE number is:

A47530

Please ensure that this number is quoted on all correspondence.

If you need any assistance on issues relating to the EUROPRACTICE Software Service, please do not hesitate to contact us. We look forward to working with you in the future.

Yours faithfully

Laura M Cherry
EUROPRACTICE Software Service

Encl Current Version CD Rom Design Kit Library
Subscription Invoice & Information Sheet (unless being invoiced with Software Order)

EUROPRACTICE SOFTWARE SERVICE COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS

EUROPRACTICE

www.europractice-ic.com

Europractice

offers at a reasonable price:

- licensed **CADs** of world leaders
- access to design rules and technological libraries (**design kits**) for a number of nanometer and submicron (40 nm … 0.8 µm) processes, including SiGe, SOI, A_3B_5

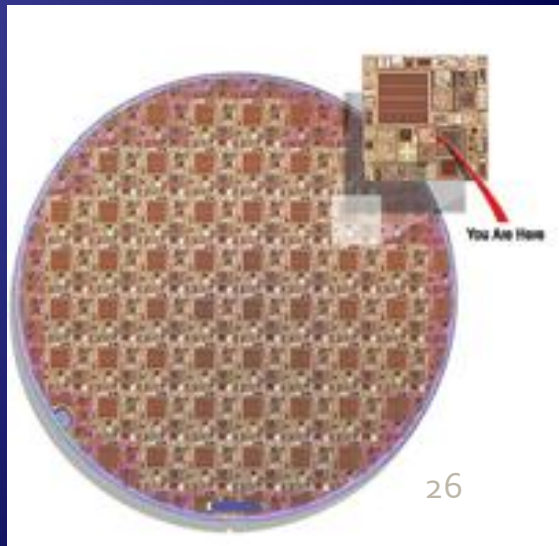
UMC tsmc ihp austriamicrosystems LFoundry ON Semiconductor

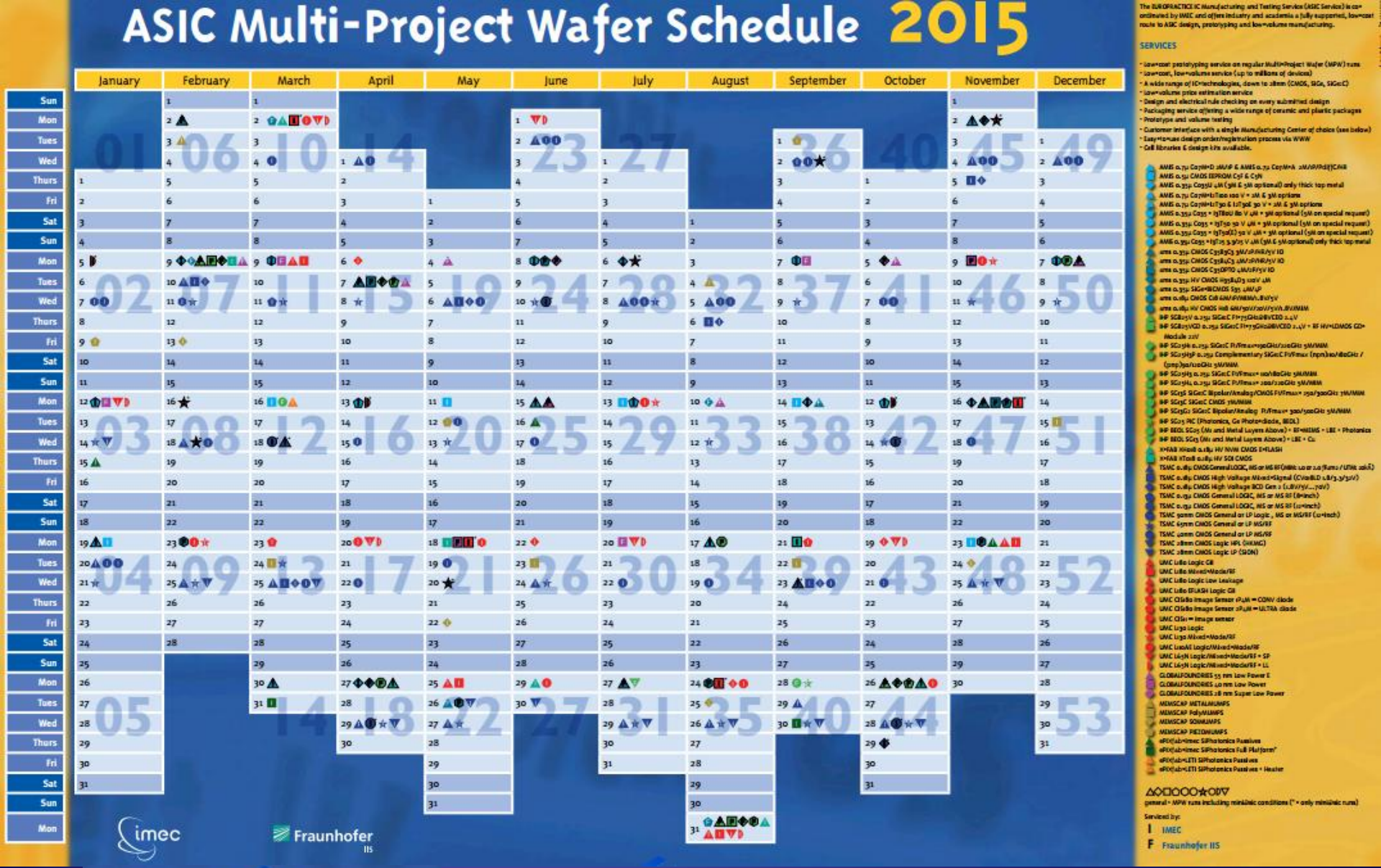
- access to **microsystem and MEMS technologies**

tronics microsystems imec MEMSCAP

provides an inexpensive (***360…7900 Euro/sq.mm***) prototyping of ASICs via advanced processes (down to **40 nm** CMOS) using the so called multiproject approach, when the wafer cost is shared among projects of many customers

since 2013 Europractice provides **discounted pricing** for Russia as well as EU

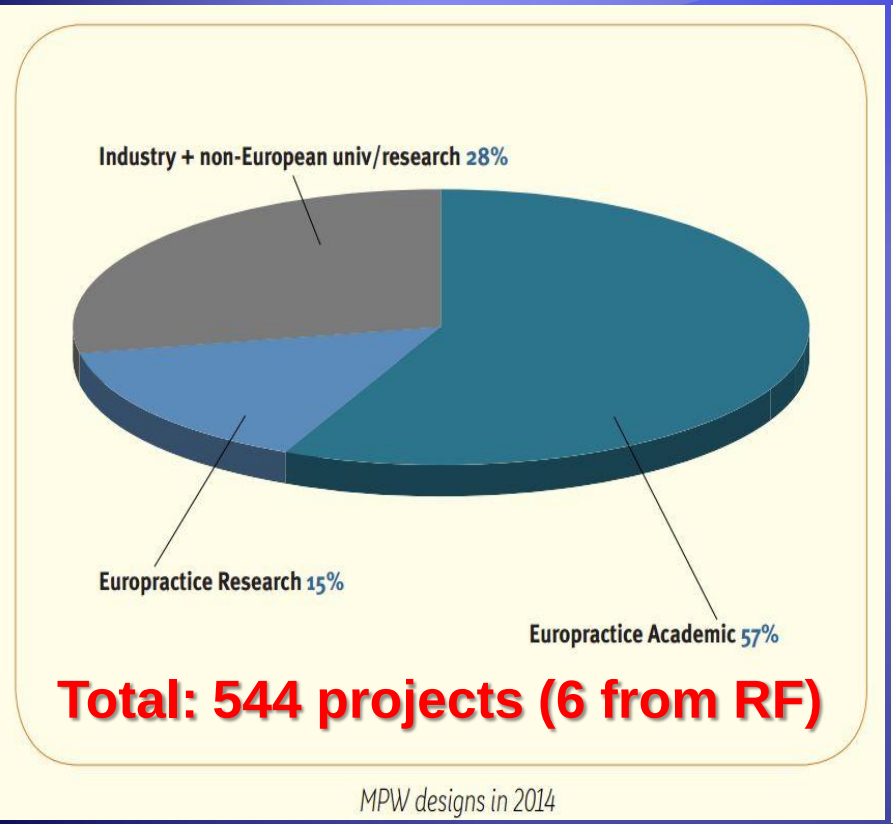




EUROPRACTICE
ASIC SERVICE

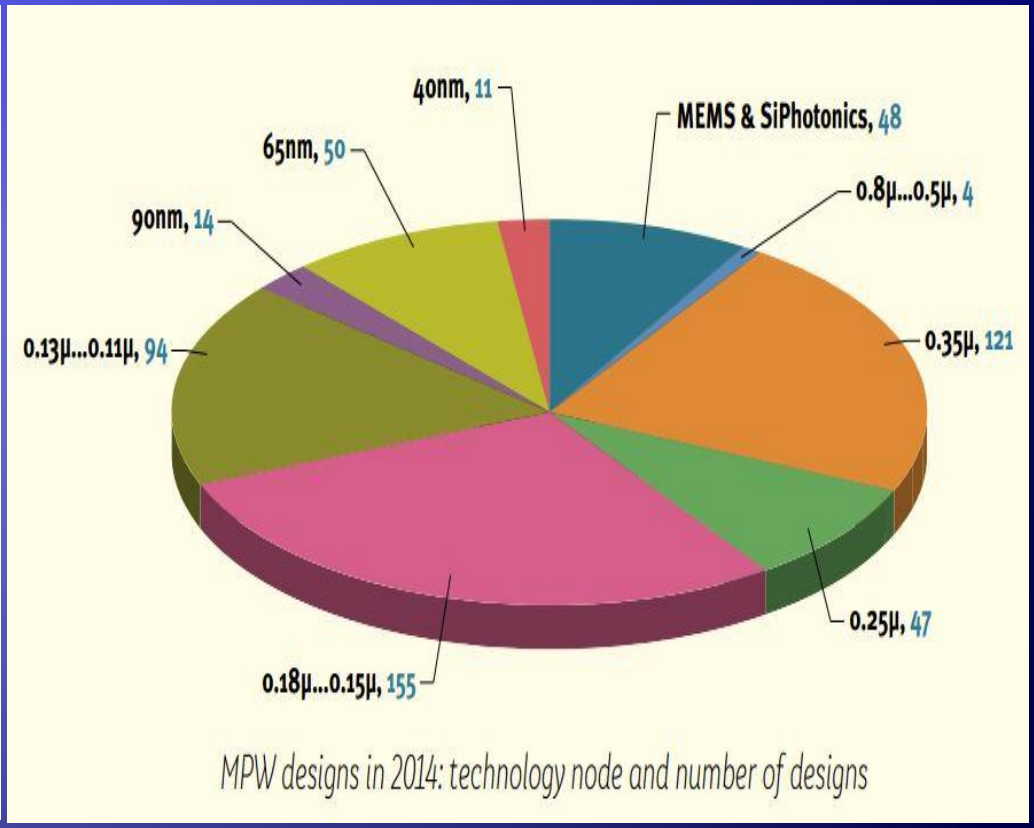
http://www.europractice-ic.com/docs/EP_wall_calendar_2015.pdf

Number of ASIC projects, manufactured via Europractice *



Total: 544 projects (6 from RF)

MPW designs in 2014



MPW designs in 2014: technology node and number of designs

* Europractice annual report 2014, www.europractice-ic.com/docs/Annual_report_2014.pdf

Number of Russian ASIC projects, manufactured via Europractice *

Russia

Budker Institute of Nuclear Physics	Novosibirsdk	3
IPMCE	Moscow	3
JSC "NTLAB"	Moscow	2
Moscow Institute of Electronic Technology	Moscow	5
Moscow Institute of Physics and Technology	Moscow	5
Moscow Engineering Physics Institute	Moscow	17
N.I. Lobachevsky State Univ	Nizhni Novgorod	8
SRIET-SMS CJSC	Voronezh	6
University St Petersburg	St Petersburg	5
Vladimir State university	Vladimir	1

* Europractice annual report 2014, C.38
www.europractice-ic.com/docs/Annual_report_2014.pdf

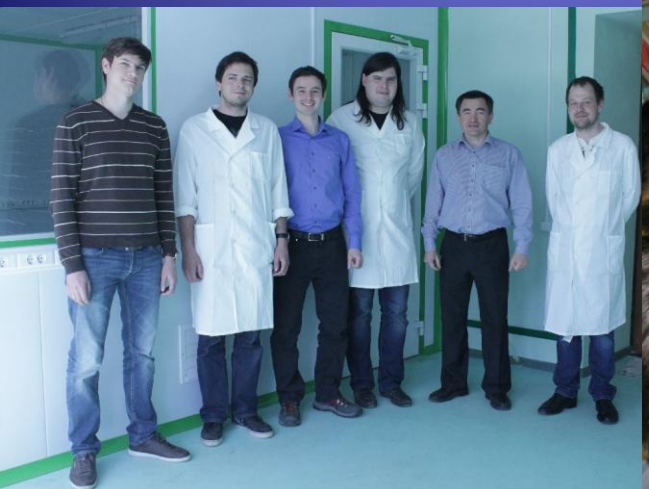
MEPHI ASIC Lab tasks

The infrastructure is financed since 2013 by a grant given by the Russian Federation Government based on resolution **№220**. The head of Lab is V. Samsonov

- Development Russian design center of Application Specific Integrated Circuits with technological nodes of 40-180 nm.
- Design of ASICs for well recognized International and Russian experiments (for ex. CBM, NIKA)
- Development of competence center on chip design. Organizing topical Conferences, Workshops, Master classes.
- Research of new project solutions, test prototyping and small volume production

Infrastructure of the ASIC design center

- distributed interdepartmental **1 Gb/s** local Intranet
- clusters of network SUN and Linux **workstations** in a number of departments
- licensed microelectronics tools for computer aided design – **Cadence, Mentor Graphics, Synopsys, Agilent**
- **computer classes** for core students
- technological libraries (Design Kits) starting from **40 nm**



Organization of All-Russia Workshops

- AMS Methodology Kit Workshop

22-24 September 2009

- II Workshop on mixed-signal IC design

10 - 14 October 2011

- Youth school on CAD tools for mixed-signal IC design for physical instrumentation

11 - 14 September 2012

- IV Methodology Workshop on CAD tools for mixed-signal IC design for physical instrumentation

29-31 October 2013

- V Methodology Workshop on CAD tools for mixed-signal IC design for physical instrumentation

8-11 December 2014

Partners:

2012 event photo

2013 event

IV Всероссийский научно-методический семинар по средствам проектирования интегральных микросхем для аппаратуры физического эксперимента

29-31 октября 2013 года

Приглашаем вас принять участие в работе семинара.

Семинар организован НИЯУ МИФИ при поддержке Минобрнауки РФ (в рамках мероприятий по Постановлению Правительства РФ №220), американской компании Cadence Design Systems (www.cadence.com) и Центра ФАИР-Россия (ИЦФР, frrc.itep.ru).

Цель семинара - познакомить участников с методологией автоматизированного проектирования смешанных (аналого-цифровых) интегральных микросхем, развиваемой компанией Cadence, и провести практические мастер-классы с целью популяризации микроэлектронных САПР для предприятий высокотехнологичного сектора экономики РФ. Приоритет будет отдан предприятиям ГК "Росатом", осуществляющим крупные проекты, такие как на международных ускорителях ФАИР (г. Дармштадт, Германия) и НИКА (г. Дубна).

Важная часть семинара - тематические лекции приглашенных известных в мире ученых из CERN (Женева), GSI (Дармштадт), AGH (Краков), отражающие последние мировые достижения в области реализации и внедрения сложнофункциональных интегральных микросхем для аппаратуры физического эксперимента.

Более подробная информация представлена на сайте: cad.mephi.ru.

ASIC projects

- 128-channel prototype ASIC for data-driven read-out of CBM STS

  0.18 um CMOS UMC (Taiwan), consumption 2 mW/ch., shaping time 100 ns, structure 128→16/ Chip contains preamplifier, shaper (filter), comparators, cross-point switch, peak detectors, 9-bit ADC and so on

- Smart sensor readout ASIC (Rosatom)

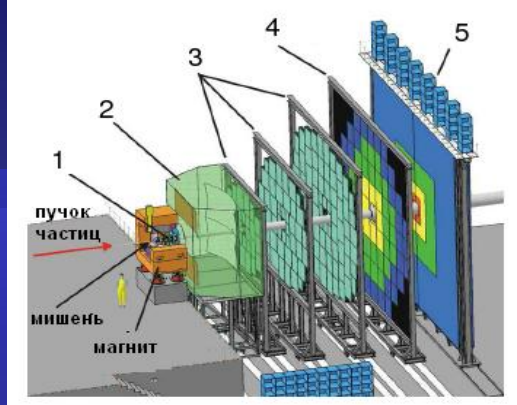
  0.35 µm SiGe BiCMOS AMS (Austria), temperature range -55…+80 ℃, consumption 3 mW. Chip contains instrumentation amplifier, 14-bit ADC, two 14-bit DAC, references, electronic termometer and so on

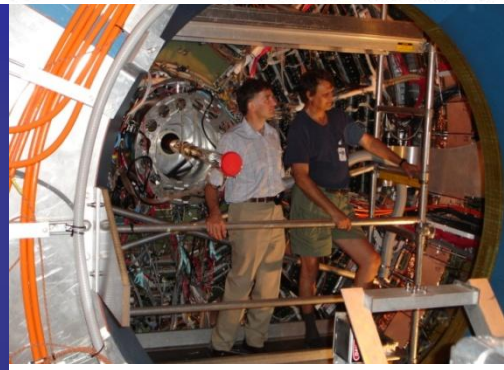
- 32-channel ASIC for "Nucleon" project (Roscosmos)

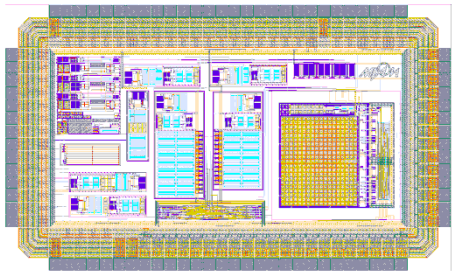
  0.35 µm CMOS AMIS/OnSemi (Belgium), dynamic range 100 pCb, consumption 2 mW/ch., multiplexed (serial) output

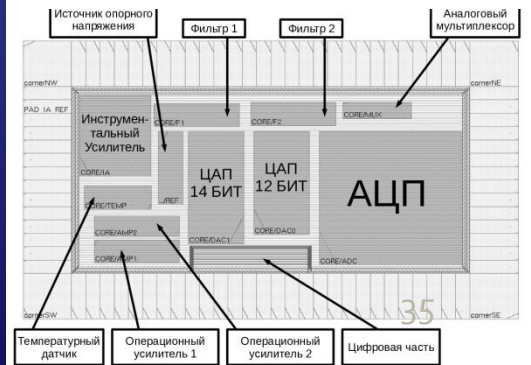
- IP blocks for system on chip, controlling a new aircraft engine (Ministry of Education and Science)

  0.18 um CMOS UMC (Taiwan), consumption 10 mW/ch., 9-bit ADC

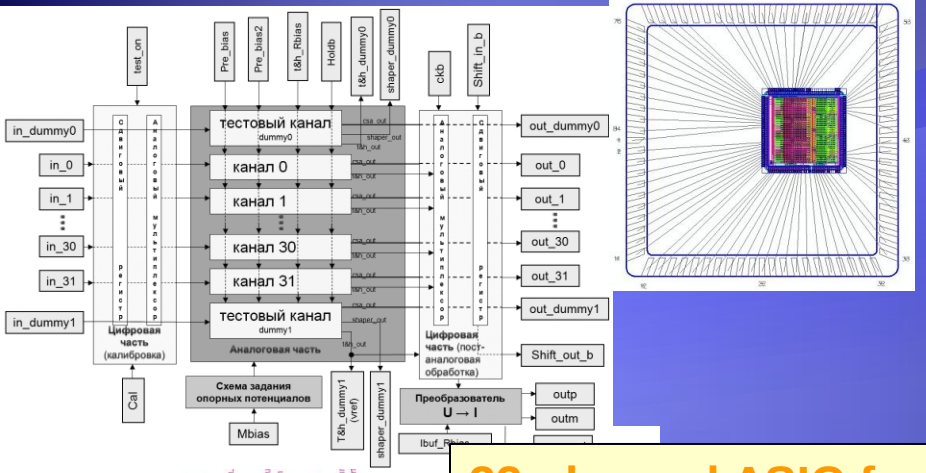


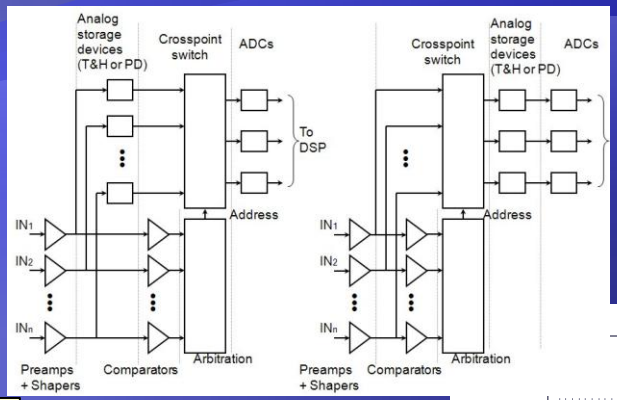


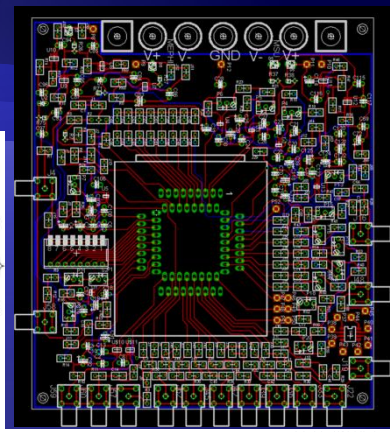




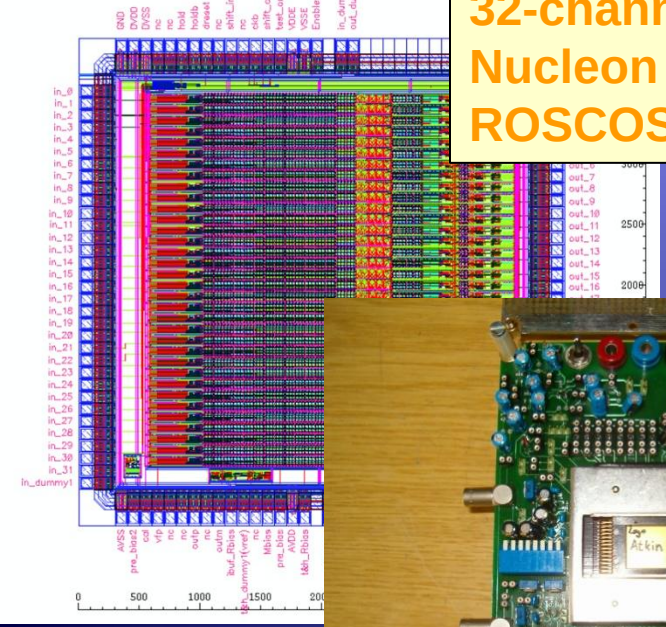
SOME DETAILS OF ASIC PROJECTS



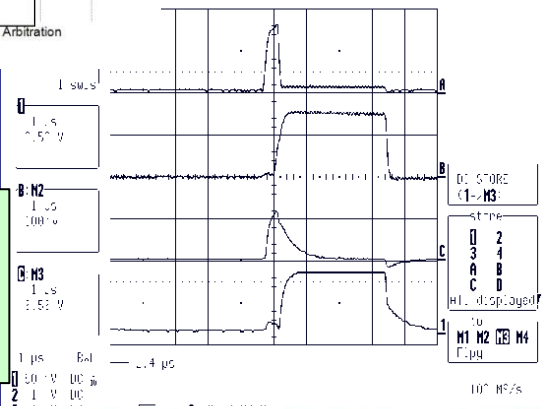


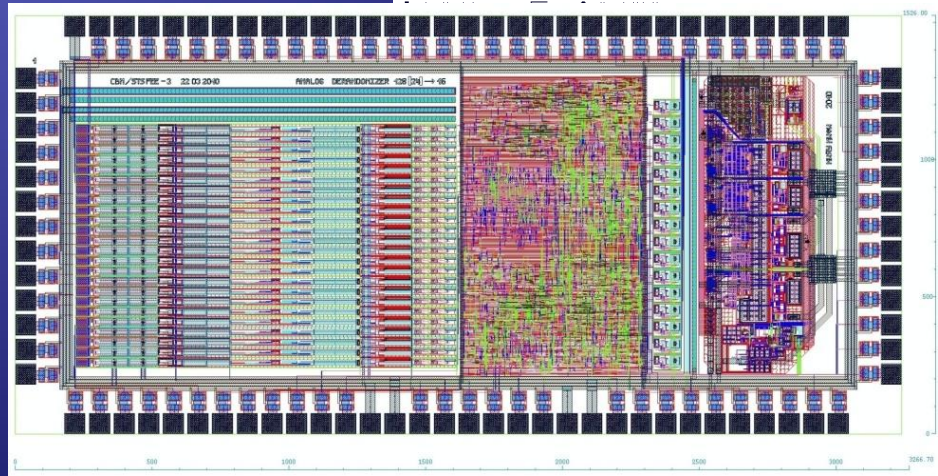


32-channel ASIC for Nucleon project of ROSCOSMOS



128-channel prototype ASIC for CBM STS





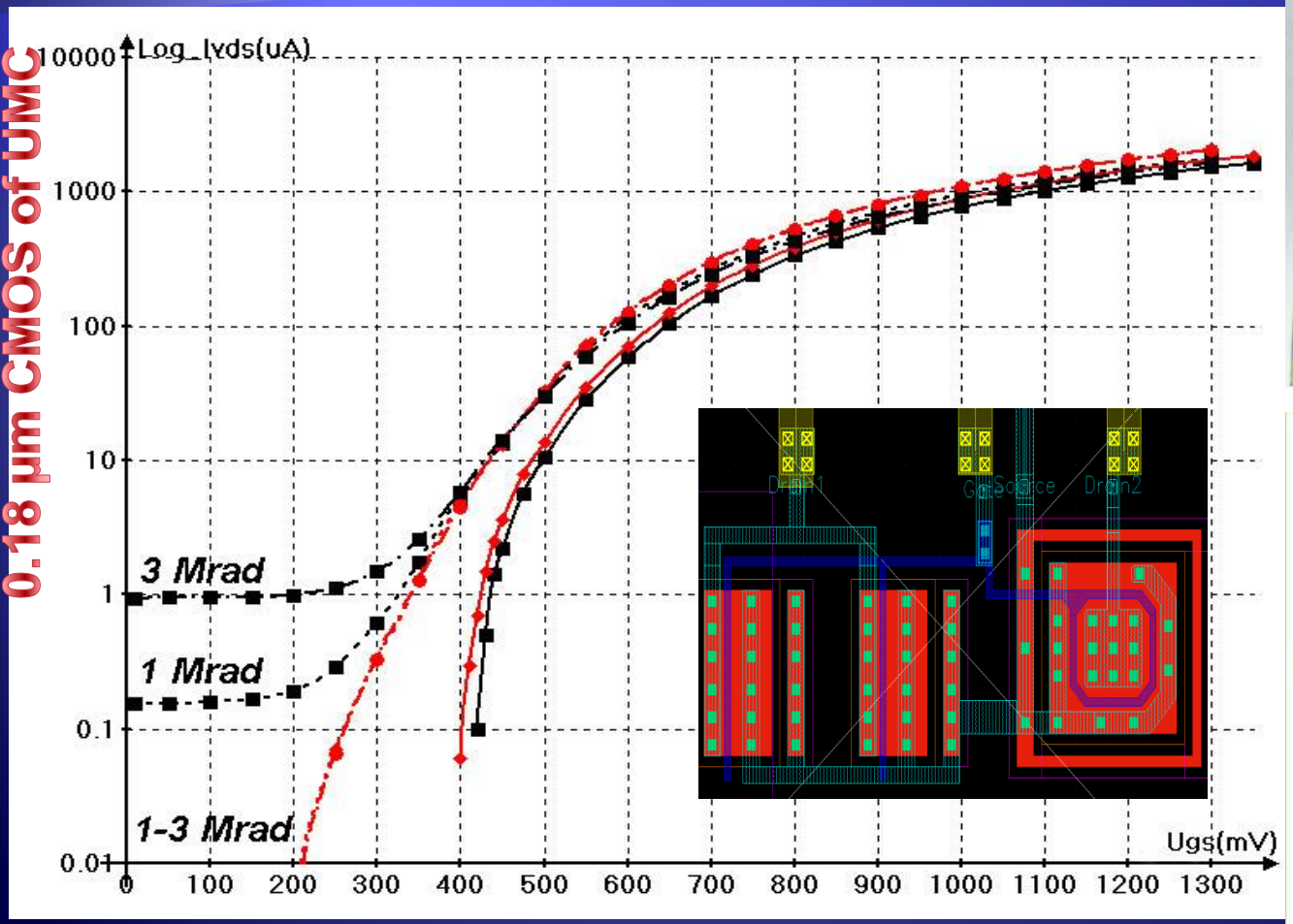
Tests for total dose effects

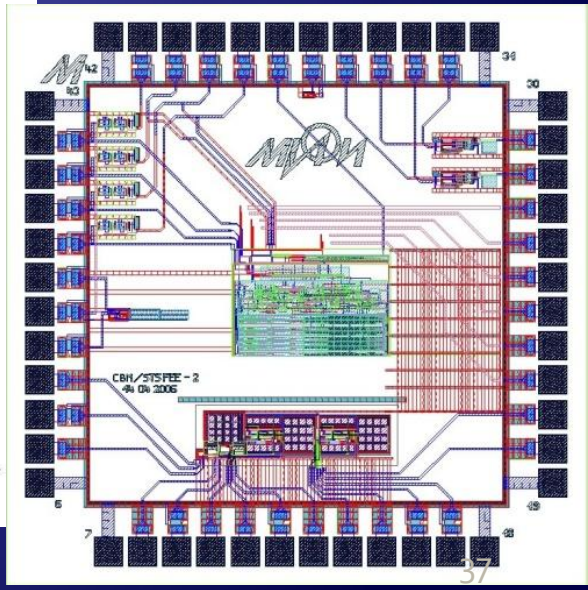
(E=8 MeV; F=10^{11} e/cm^2 s; D=0.1; 1; 3 Mrad)

1) Threshold voltage shift (~100 mV);

2) Leakage currents --- standard (strip-like) nMOS;

--- ring transistors

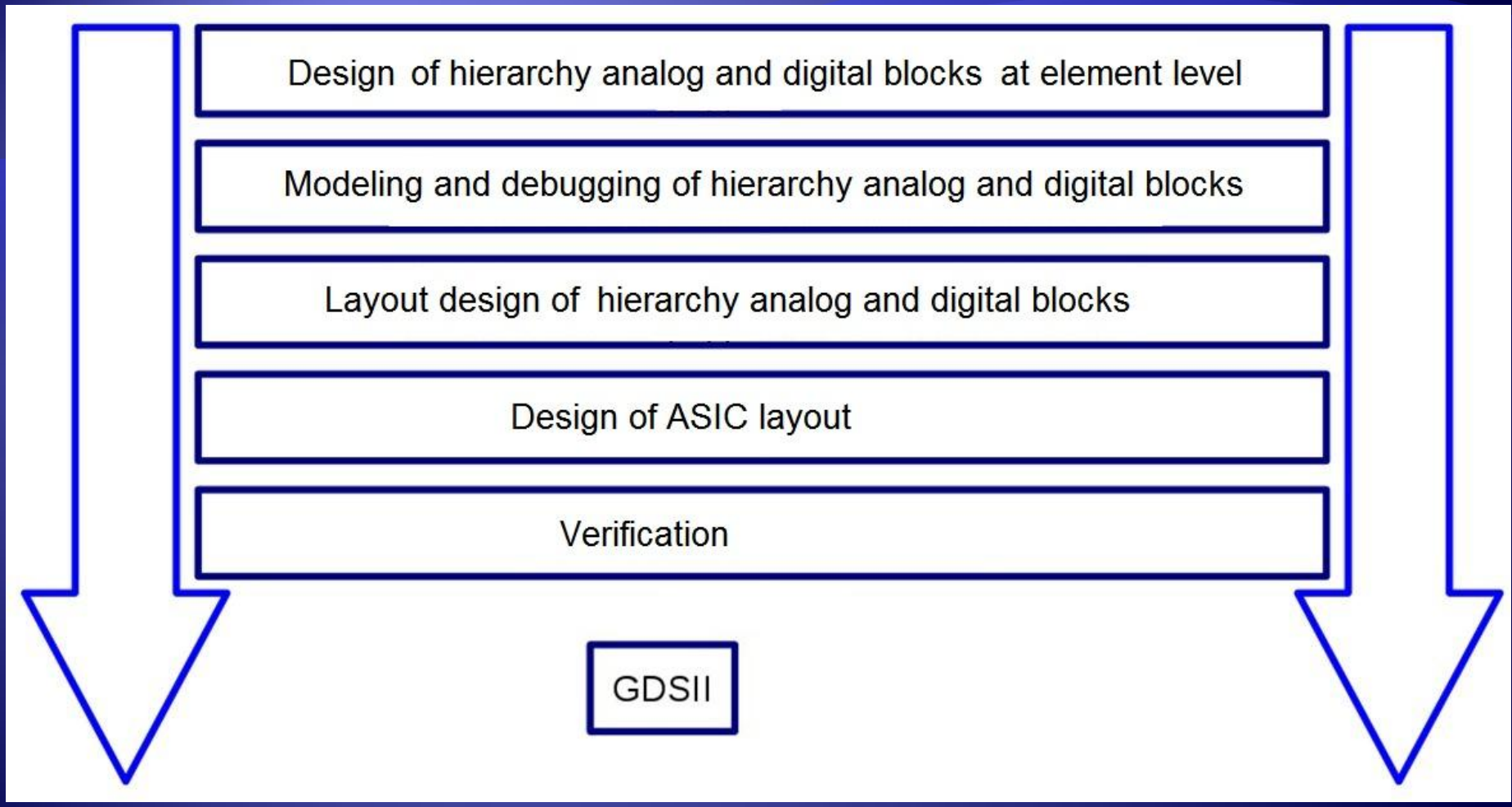




5 design phases for ASIC development

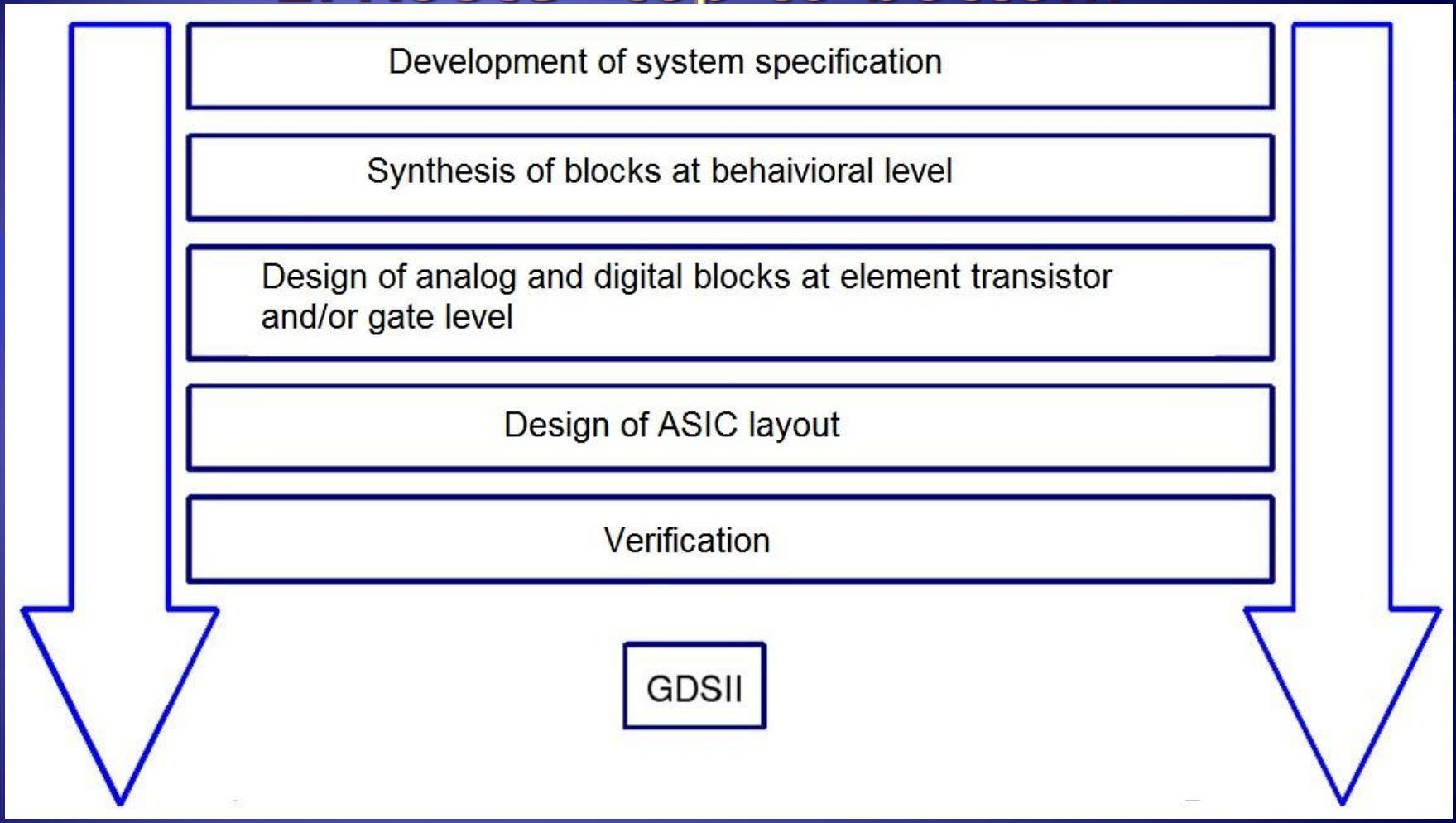
- Phase I: Design of analog and mixed-signal ASICs
- Phase II: Prototyping and test technique development
- Phase III: First tests and prototype characterization
- Phase IV: Qualification of ASICs
- Phase V: Preparation for a batch production and testing automation

1. Route «bottom-to-top» (traditional)



Feature: the possibility to perform a mixed-signal simulation for analysis of blocks interaction appears only after the all separate blocks being ready

2. Route «top-to-bottom»



Feature: the usage of mixed-signal simulations at early stage. Due to system synthesis at structure level, it becomes possible to develop fastly the block descriptions at behavioral level – RTL-Verilog, Verilog-A и Verilog-AMS. The same level of abstraction is available with VHDL

General principles of mixed-signal design

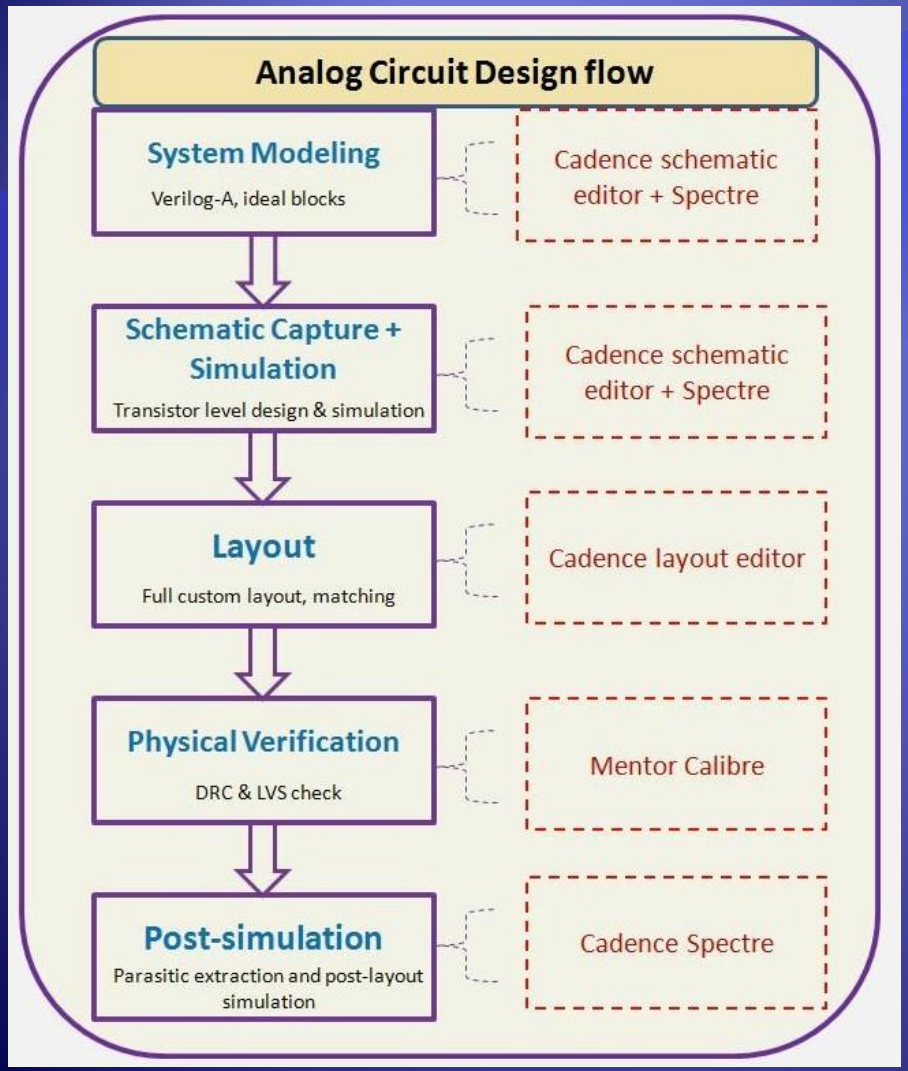
Modern ASICs, as a rule, are **mixed-signal** chips. They surely include both analog and digital parts

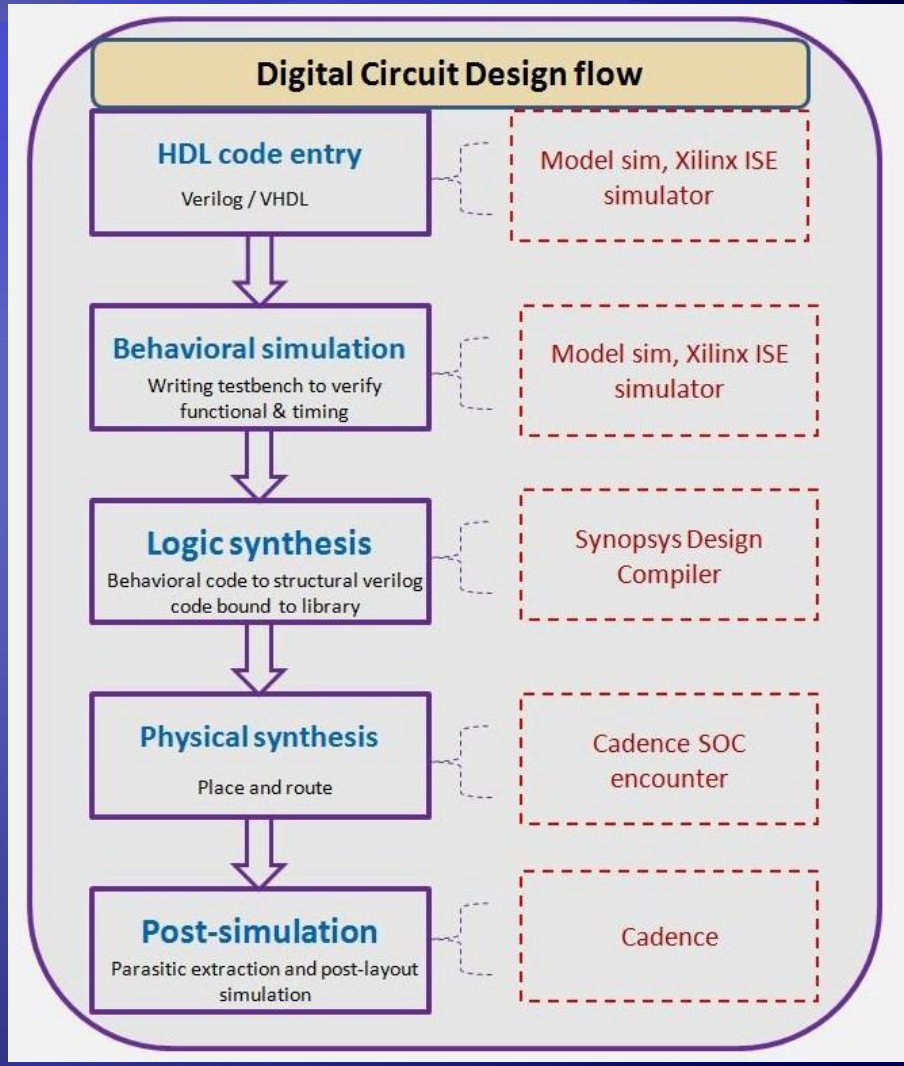
Analog part is designed as a custom block, whereas the digital one is described by VHDL or Verilog and then synthesized as a semicustom block, based on standard digital libraries

Now a system simulation at element (transistor) level requires unacceptably a lot of time

Usage of high description languages and software tools for **hierarchy** design allows to perform simulation with **different abstraction** level of blocks

Traditional design routes

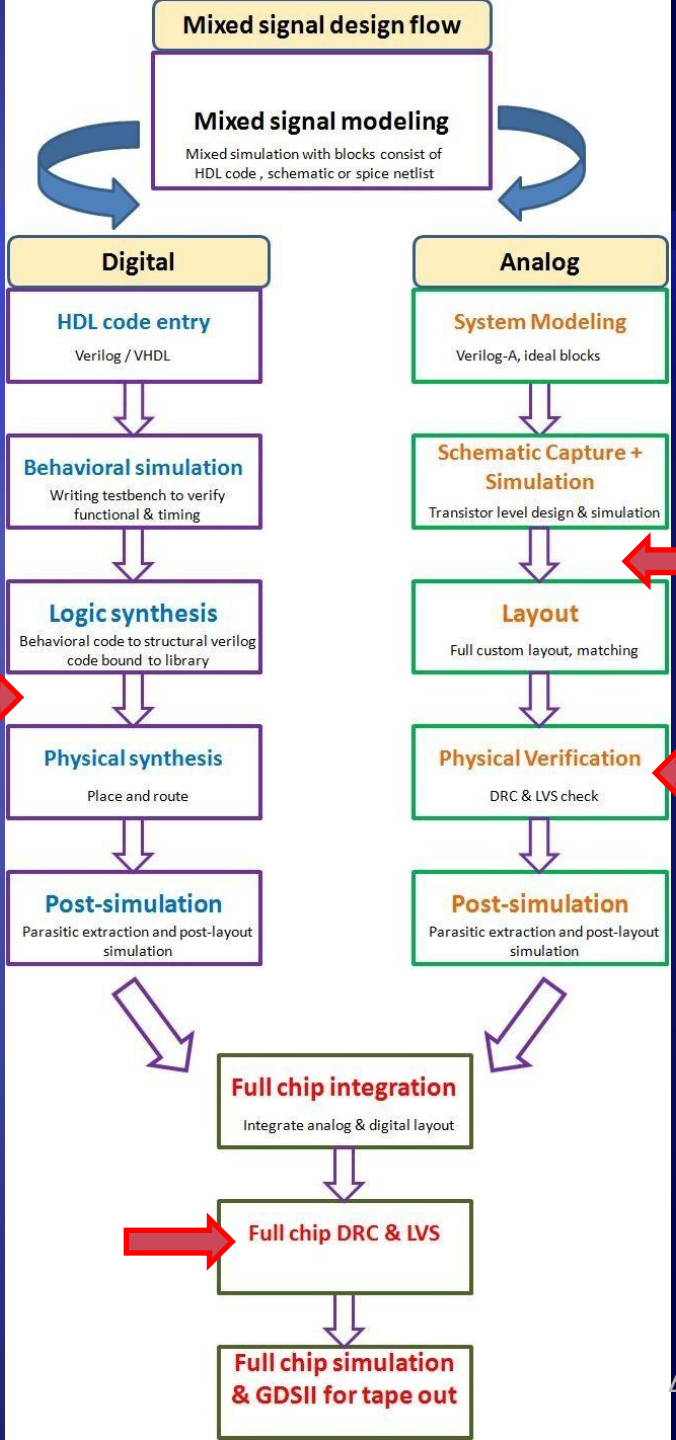




Routes for mixed-signal design

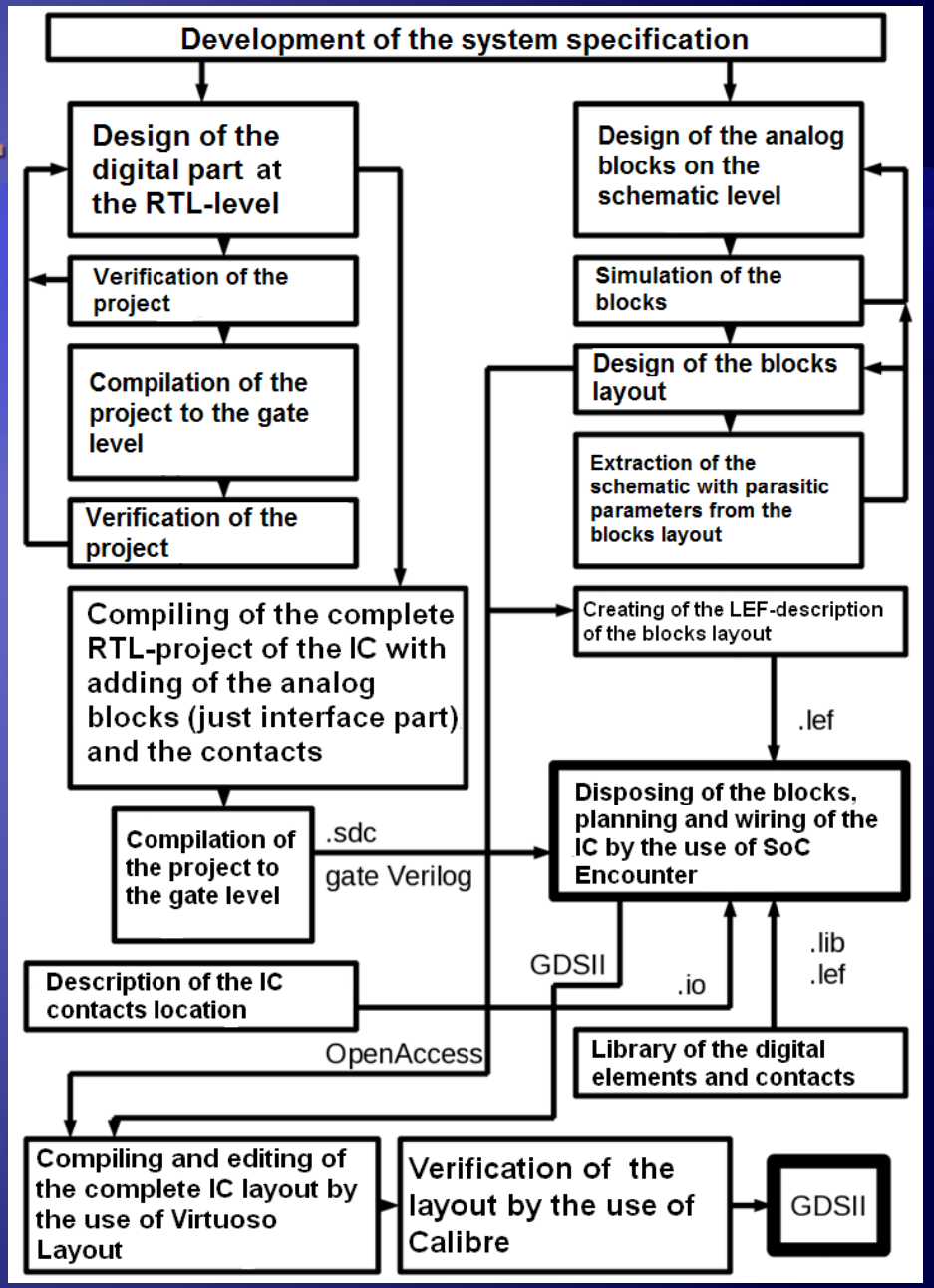
Usage of high description languages and software tools for **hierarchy** design allows to perform simulation with **different abstraction** level of separate blocks

→ Design aspects, taking into account the requirements on radiation hardness

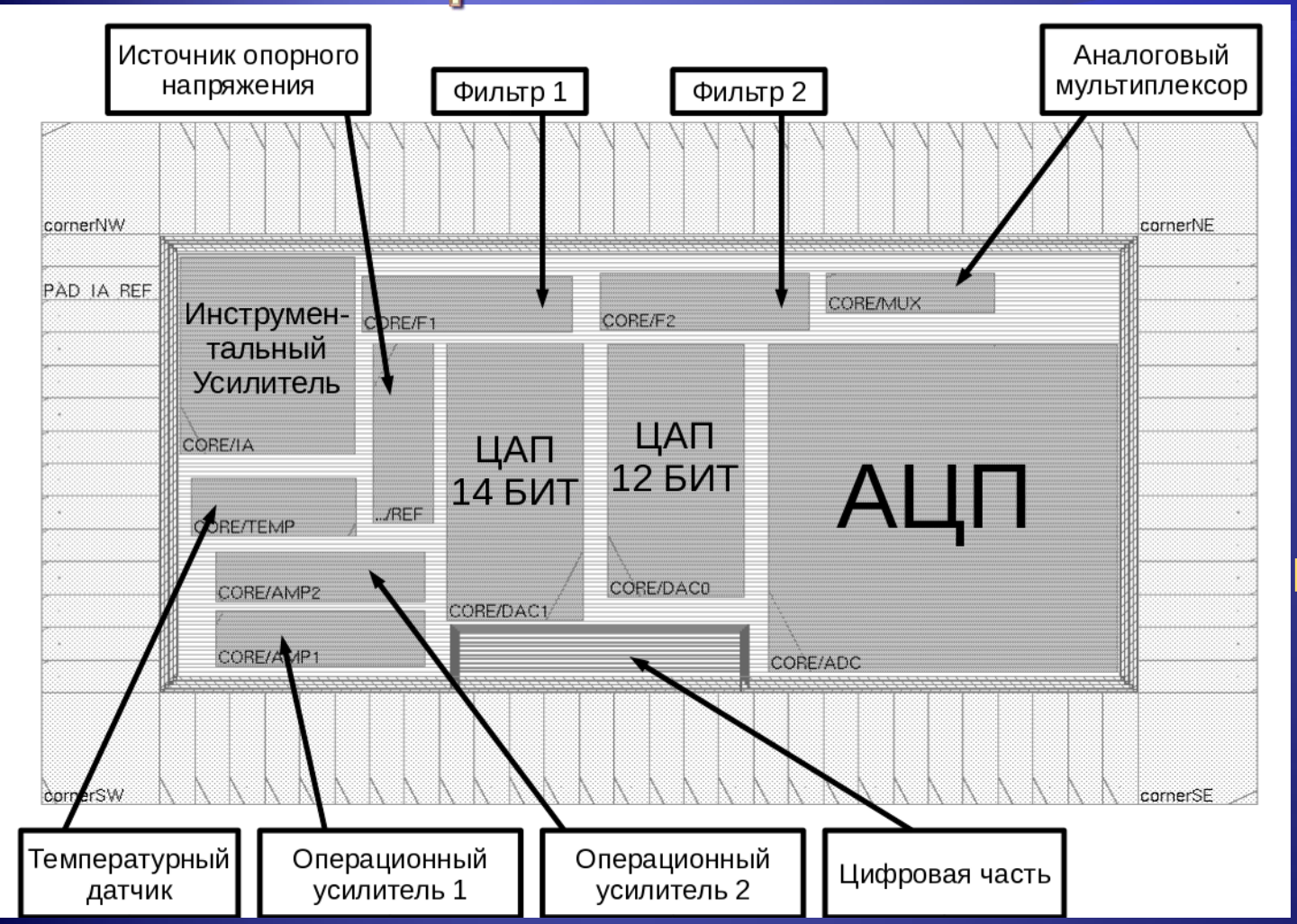


Example route for a smart pressure sensor readout ASIC

- Verilog description of whole ASIC
- Analog blocks are described as digital modules without functions, but with interface part
- Project compilation in gate level verilog
- For debugging it is necessary to have layout views of both standard library elements and analog blocks in format LEF (library exchange format)
- Few next stages are made in SoC Encounter, namely: placement of analog blocks, placement of digital part, routing of power supply buses, routing of signal wires



Smart pressure sensor readout ASIC

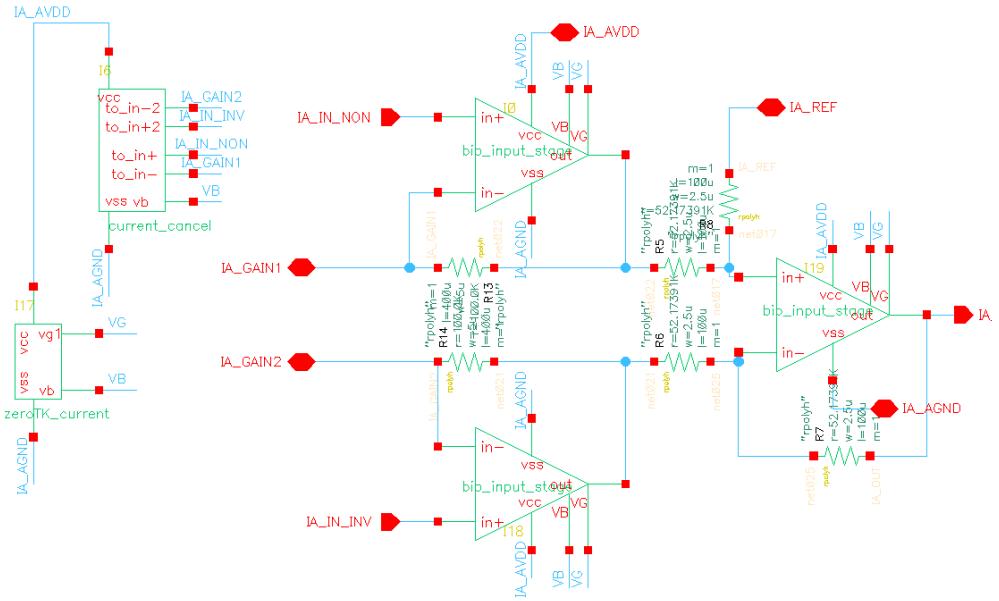


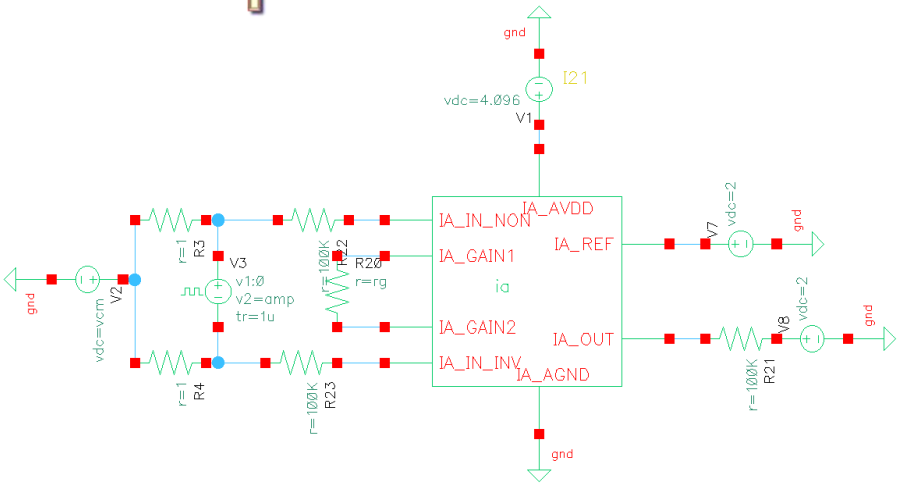
Customer – Rosatom

Design duration – 8 months of 2010

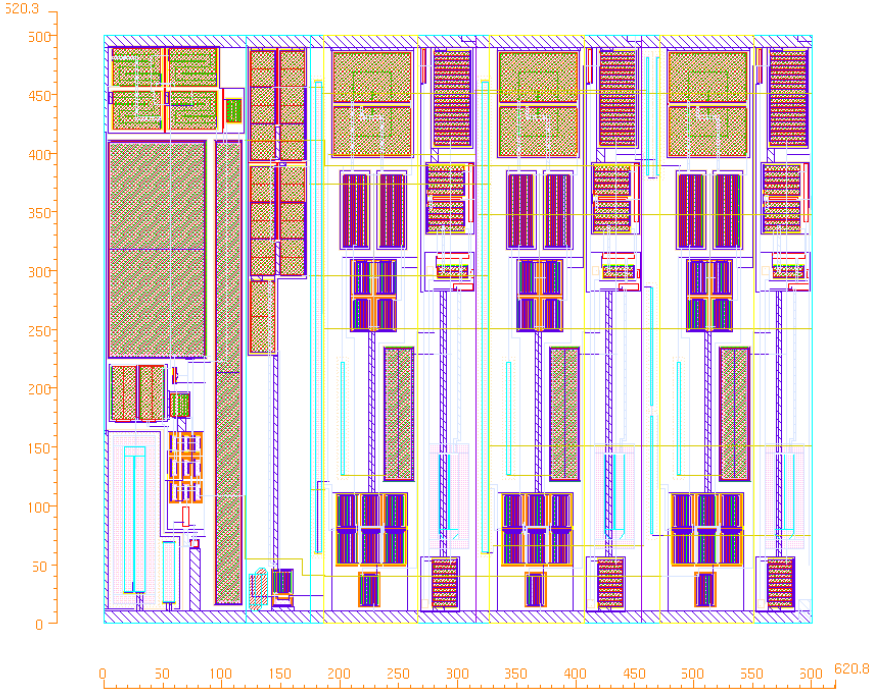
Chip planning in SoC Encounter (Cadence)

Instrumentation amplifier

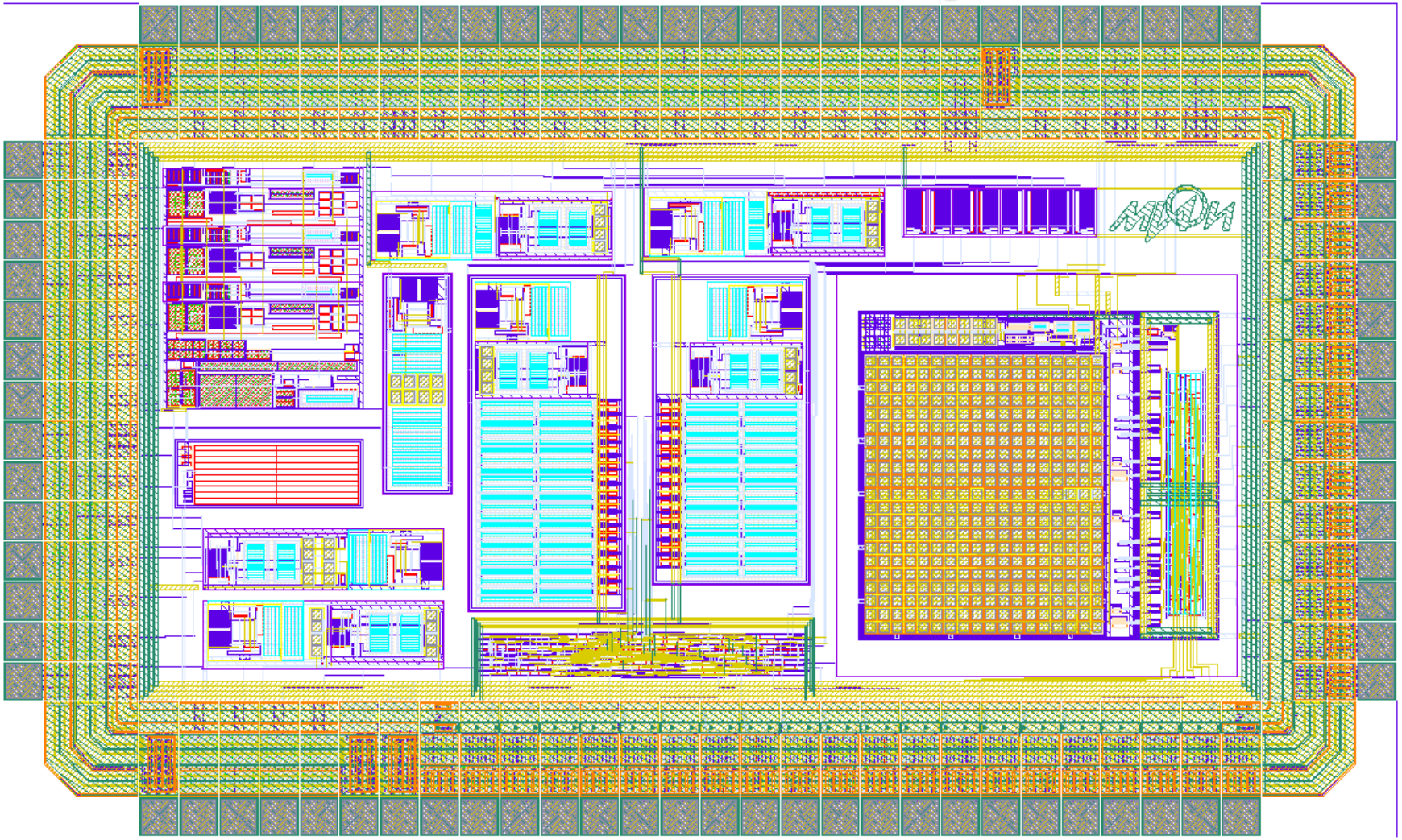




Name	IA specs
Opamp gain	96 dB
Unity gain frequency	2 MHz
Phase margin	70 degree
Consumption current	100 µA
RMS noise	20 nV/Hz$^{1/2}$
Temperature range	-55…+80 ºC
Input current	5 nA
Offset voltage	100 µV

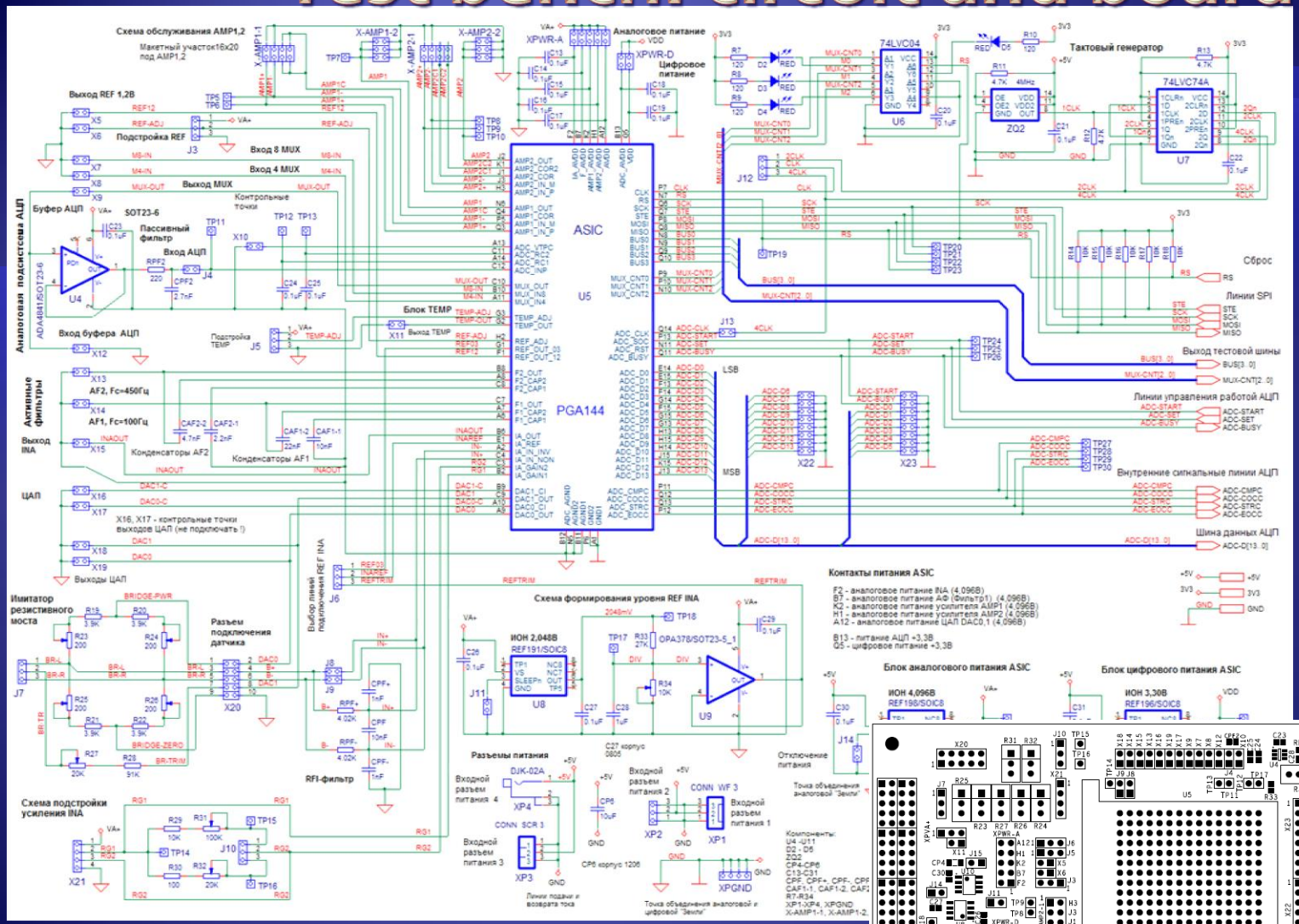


Smart sensor ASIC layout

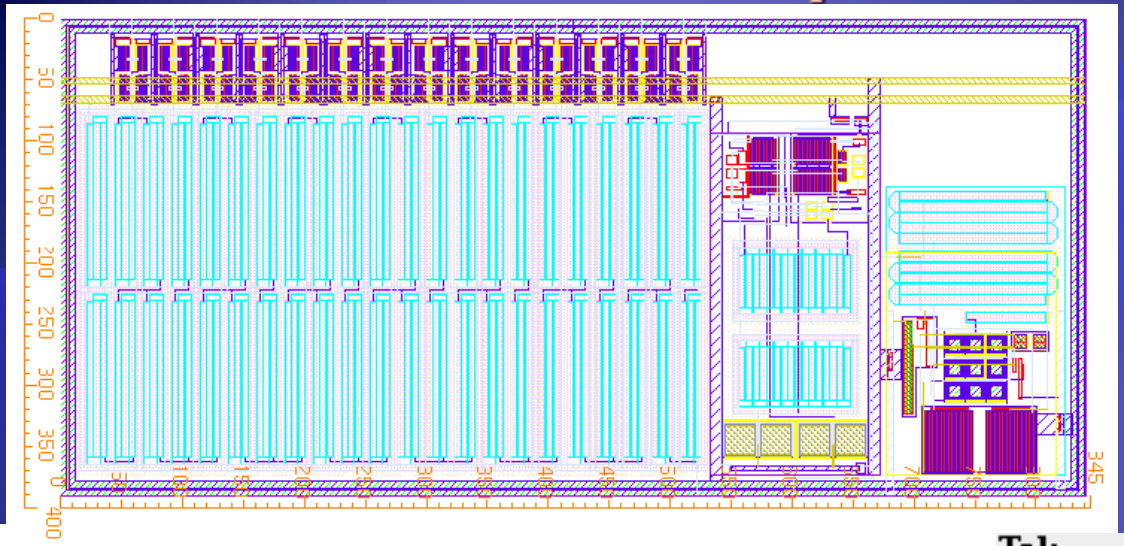


SiGe 0.35 µm BiCMOS of AMS

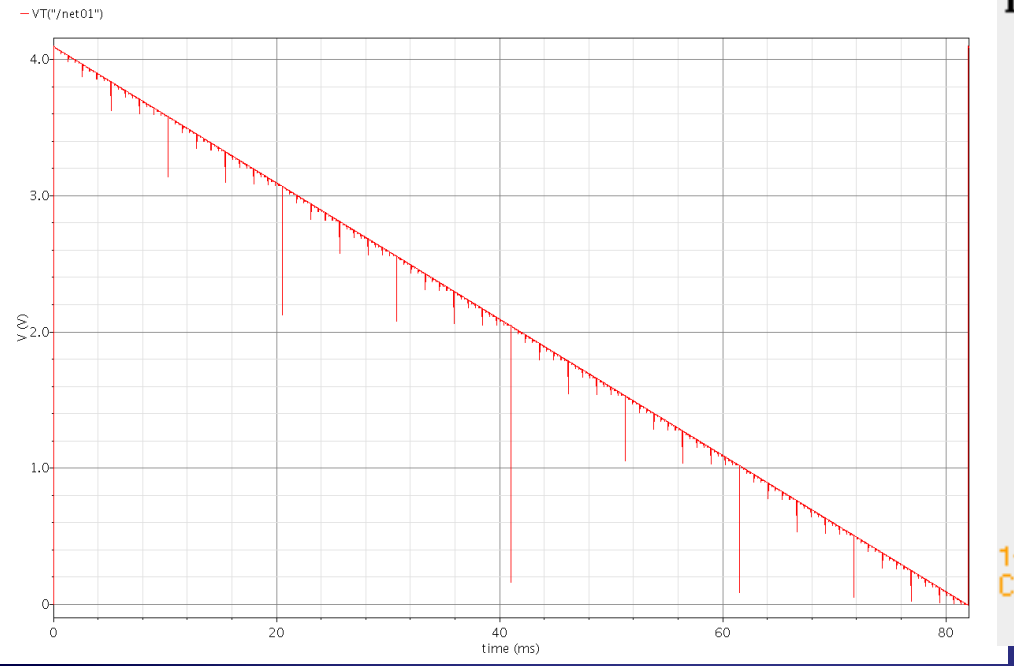
Test bench: circuit and board

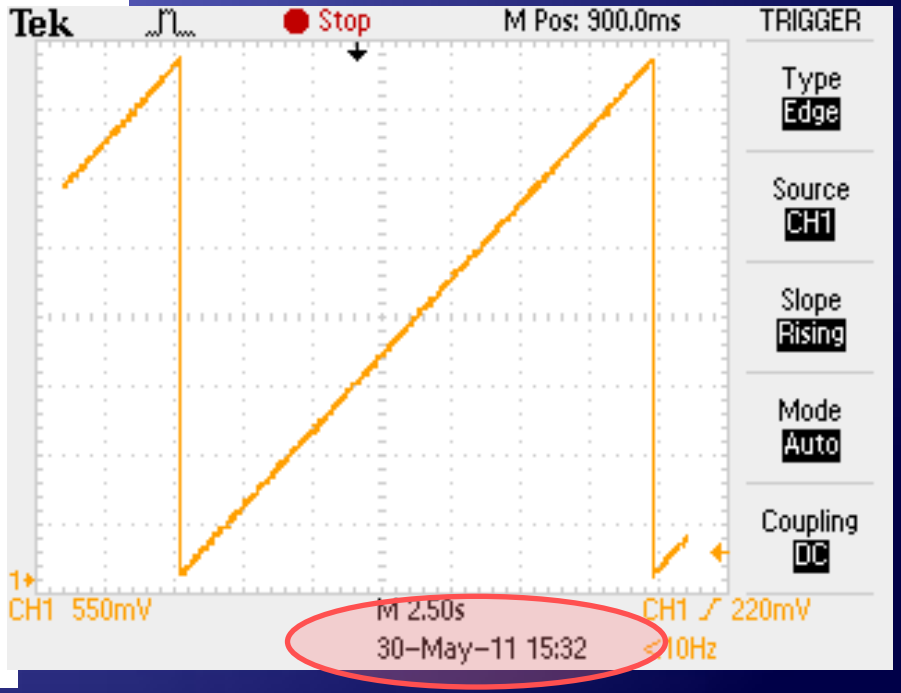


14-bit DAC

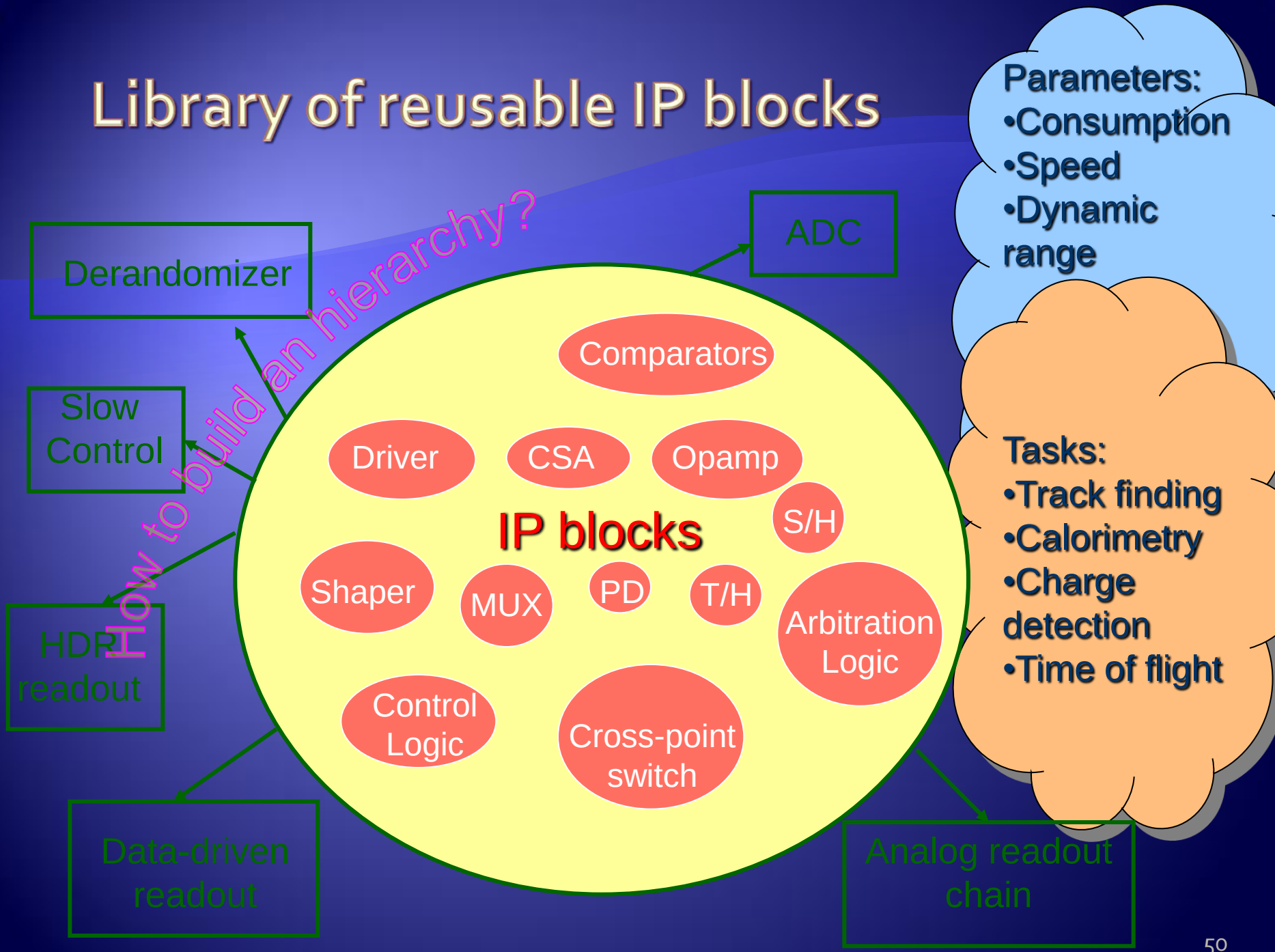


Name	DAC1
Number of bits	14 bits
Output range	3,9 V
Differential nonlinearity	1 LSB
Integral nonlinearity	2 LSB
Consumption current	80 µA





Library of reusable IP blocks



ASIC for Nucleon project*

- Large dynamic range (100pC), consumption 2mW/ch, 32 chs.
- Prototyped in 2005-2009 and reproduced in 2012
- AMIS 0.35 um CMOS process
- 6 respins:

1) Analog, 16 CSAs (включен в отчет Europractice 2005г.) Feb 2005
2) Mixed-signal, 4+2(тест.) CSA+SH+T&H+MUX+Driver Sept 2006
3) Mixed-signal, 4+2(тест.)CSA+SH+T&H+MUX+Driver Feb 2007
4) Mixed-signal, 32+2 (тест.) CSA+SH+T&H+MUX+Driver Apr 2007
5) Mixed-signal, 32+2 (тест.) (включен в отчет Europractice 2009г.) CSA+SH+T&H+MUX+Driver Sept 2009
6) Мелкосерийное производство. Mixed-signal, 32+2 (тест.) CSA+SH+T&H+MUX+Driver Apr 2012

- Late 2014 ASIC has been launched from Baikonur to the Space

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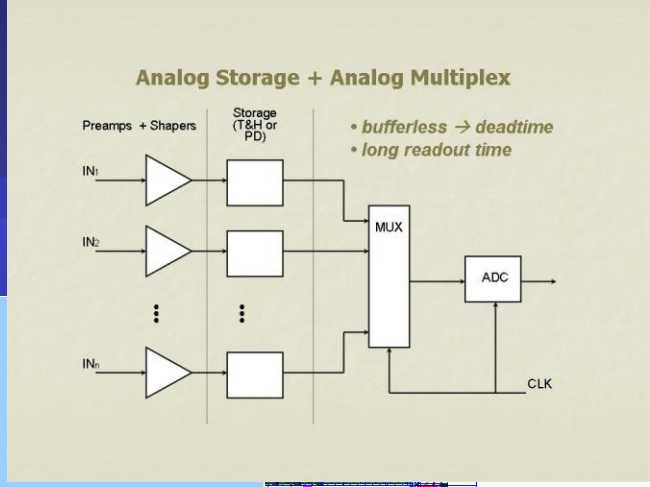
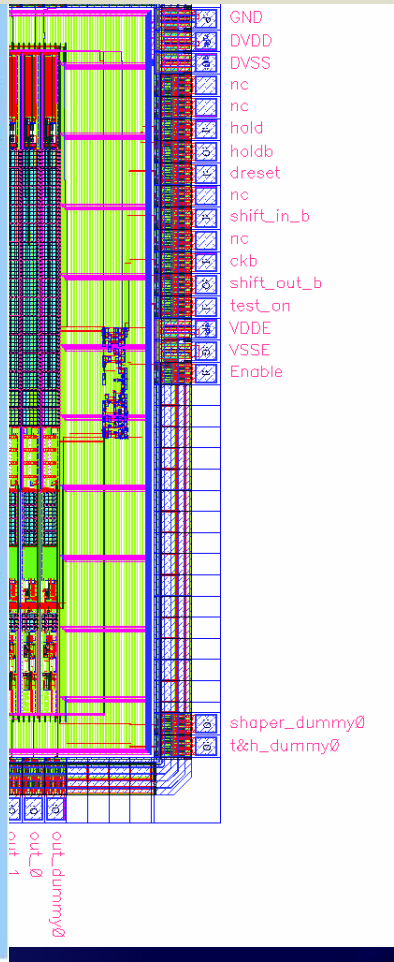
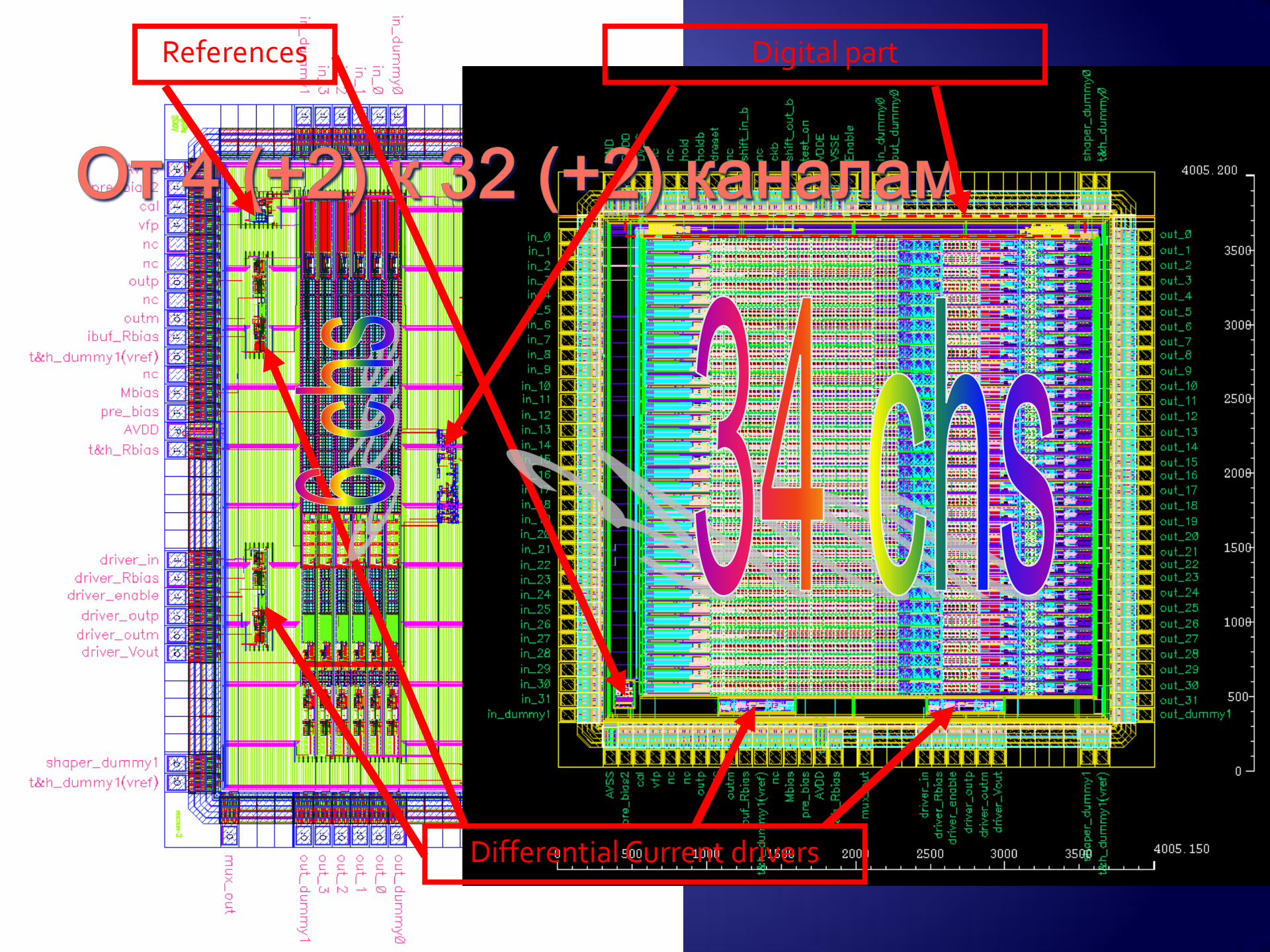
* ROSCOSMOS project (to be presented by A. Voronin)

ASIC Structure

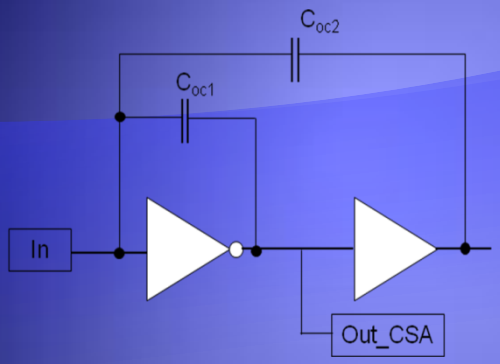


test_on
Pre_bias
Pre_bias2
t&h_Rbias
Holdb
t&h_dummy0
shaper_dummy0
ckb
Shift_in_b
in_dummy0
in_0
in_1
in_2
in_3
in_dummy1
Shift reg
MUX
Calibr.
Cal
Test channel 0
Channel 1
Channel 2
Channel 3
Channel 4
Test channel 1
csa_out
shaper_out
t&h_out
Analog chain
Bias block
Mbias
T&h_dummy1 (vref)
shaper_dummy1
Shift reg.
MUX
out_dummy0
out_0
out_1
out_2
out_3
out_dummy1
Shift_out_b
Convertion U → I
outp
outm
mux_out
Ibuf_Rbias

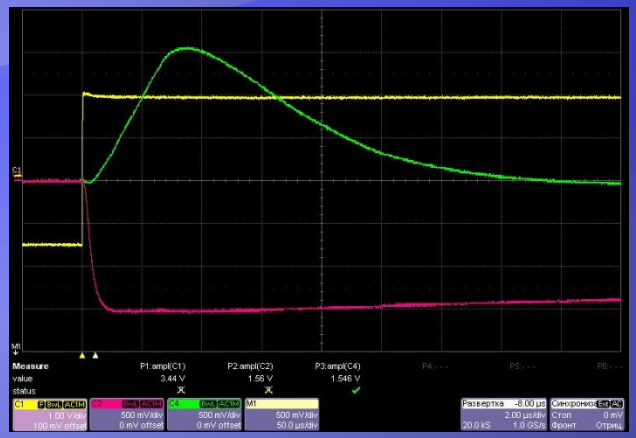



References
Digital part
От 4 (+2) к 32 (+2) каналам
16 ch
34 ch
Differential Current drivers

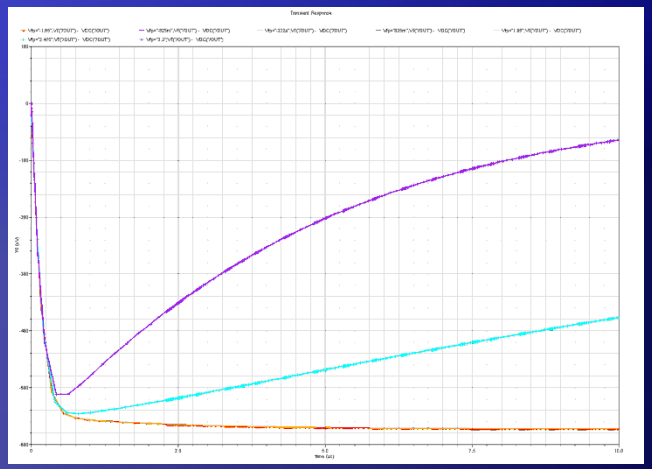
Scope diagrams



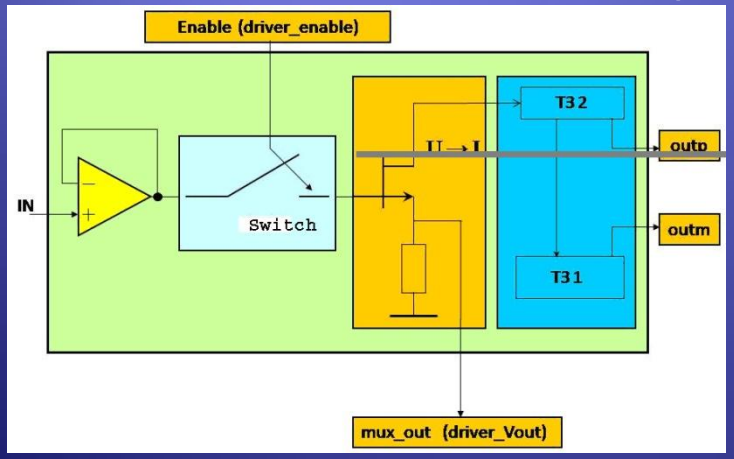
CSA structure



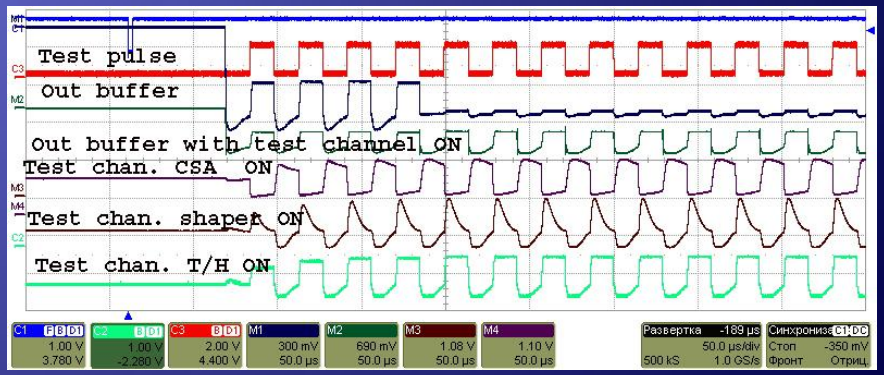
CSA/shaper response



CSA tail adjustment



Output current driver



Typical waveforms

Some relevant references

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3. A.Marchioro, Can HEP Afford Private MPW Runs in the Future? // Proc. 5th international meeting on Front End Electronics for High Energy, Nuclear, Medical, and Space Applications, Colorado, 2003 http://www-ppd.fnal.gov/EEDOffice-w/conferences/FEE_2003/FEE2003talks/E4_Marchioro.pdf
4. Europractice annual report 2014. www.europractice-ic.com/docs/Annual_report_2014.pdf
5. R. Lacoe, Improving Integrated Circuit Performance Through the Application of Hardness-by-Design Methodology IEEE Transaction on Nuclear science, v. 55, N4, 2008, p.1903-1925
6. K.Roy, B.Jung, A.Raghunathan, Integrated systems in the more-than-Moore Era: Designing lowcost energy efficient systems using heterogeneous components/ 23rd International Conference on VLSI Design, 2010

Some relevant references (II)

7. Marchioro A Microelectronics for Instrumentation in Physics 2012 Proc. All-Russian Workshop on Electronics at MEPhI

8. Snoeys W Microelectronics for Instrumentation in Physics 2013 Proc. All-Russian Workshop on Electronics at MEPhI

9. Haller G et al. 2013 *arXiv: 1307.3241*

10. RD Collaboration Proposal 2013 CERN-LHCC-2013-008 / LHCC-P-006

11. Marchioro A 2015 *Proc. of TWEPP-2015*

12. INTEL 2012 Moore's Law: Fun Facts *http://www.intel.ru/content/www/ru/ru/history/history-moores-law-fun-facts-factsheet.html*

13. White M and Bernstein J B 2008 JPL Publication 08-5, *https://nepp.nasa.gov/files/16365/08_102_4_%20JPL_White.pdf*

Conclusions

The future of particle physics ans astrophysics instrumentation is tightly bound with a wide usage of **ASICs** due to the new challenge in integration scale

The solution of **system** (architectural, structural) problems will demand substantially higher efforts. Actually there is the question of creating not separate components, but whole systems on chip (**SoC**)

Almost all new chips have a **mixed-signal character**

Nowadays the design is based on microelectronic **CADs** and the adapted **Design Kits** of the chosen manufacturer

Reduction of timelines for design, extension of reusable IP block libraries, new level of **system tests** for readout electronics – all of that requires the usage of advanced CAD in distributed fast networks of powerful computing clusters

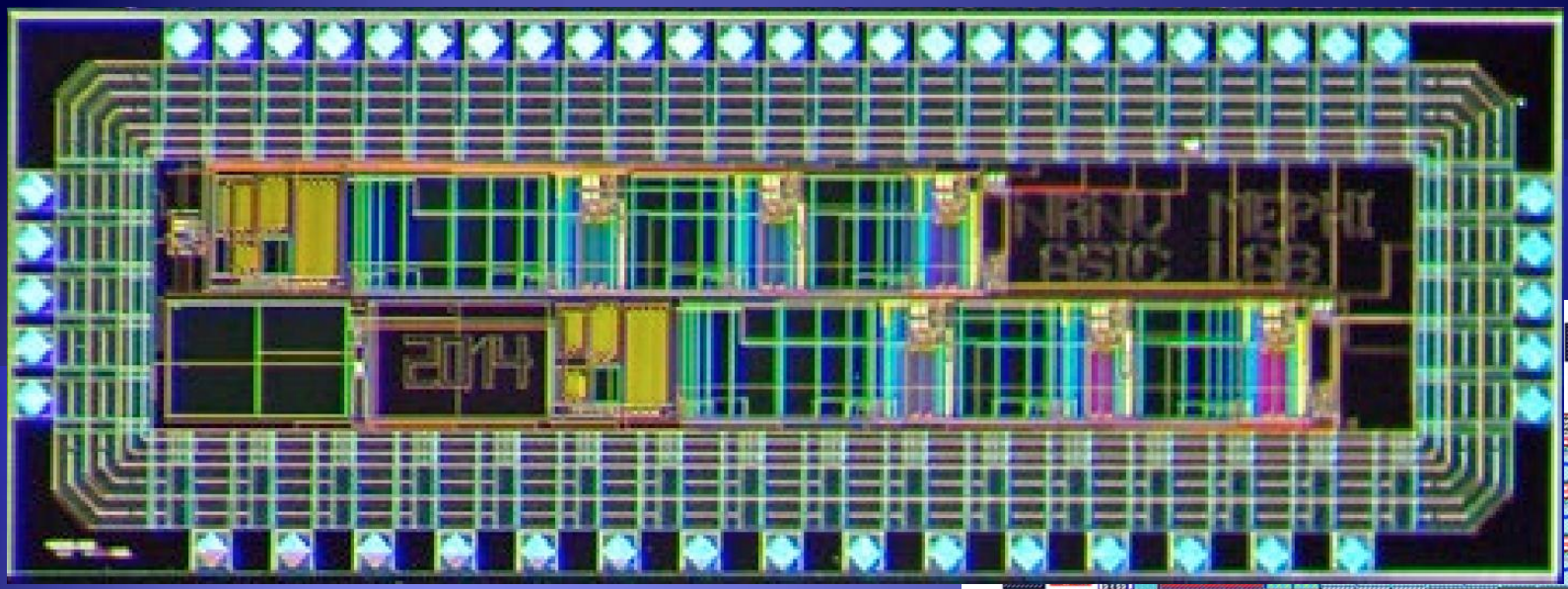
Conclusions (2)

The **"Rad-hard by design"** approach for commercial CMOS technology is considered to be the best way of providing an **acceptable** rad-hardness by circuital and layout techniques.

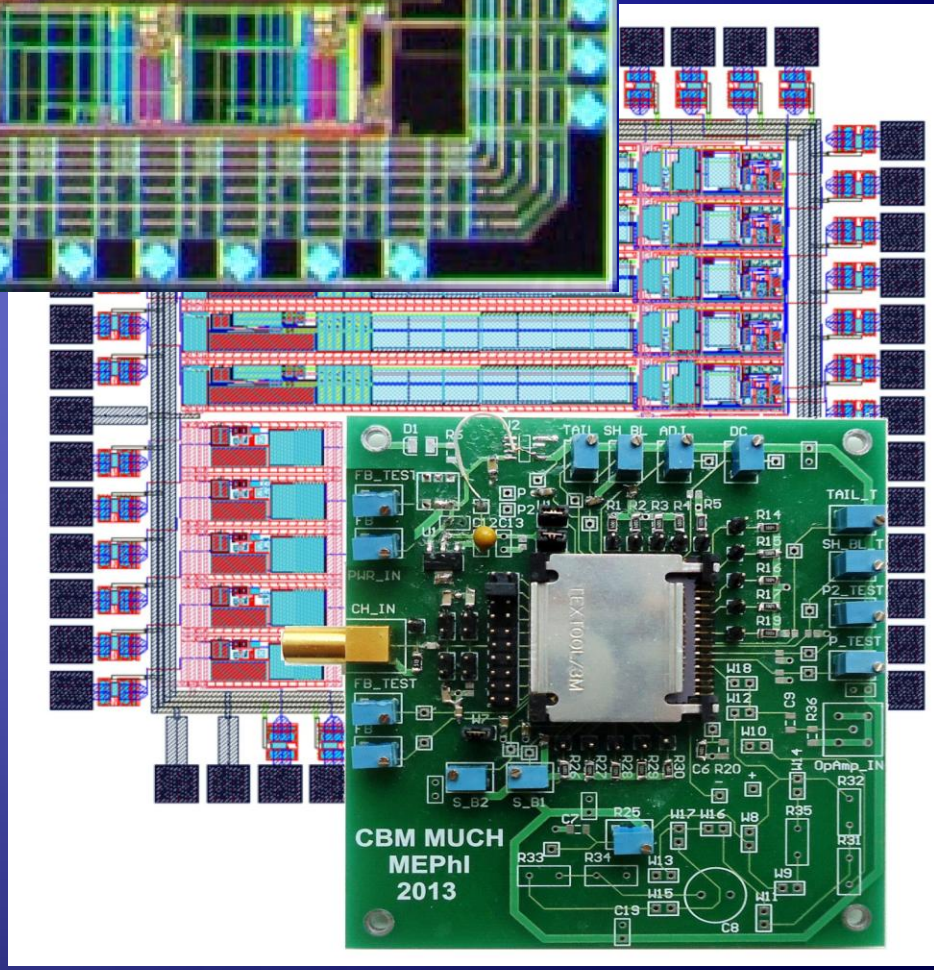
For rad-hardness and temperature stability of the chips it is important to refine the existing libraries and design routes

Long term planning becomes an extremely important factor, especially taking into account the "life time" of both the chosen technology and the design staff

The necessity of a **wider collaboration** between the design centers and research institutions, sharing the process of preparing human resources and the cost of using expensive CAD



Thanks for your attention



Back ups

- Technological level in Russia

Technological level in Russia

THE FEDERAL TARGET PROGRAM "DEVELOPMENT OF ELECTRONIC COMPONENT BASIS AND RADIOELECTRONICS" FOR 2008 - 2015

Approved by the Government on November, 26th, 2007, decree N 809

2 main target indicators:

– The **technological level** of modern electronic component basis is estimated, basing on the one of microelectronic products, mastered in manufacture

- **2008** → 0.18 μm
- **2011** → 0.09 μm
- **2015** → 0.045 μm

– There should be created 64 chip design centers in Russia

Important current tasks for Russia:

• A new Federal program on developing a chip design center network, comprising up to 150 centers, has been approved

• Creation of an advanced national photomask center