# Study of noise characteristics of irradiated pixel detectors

Dmitrii Nesterov, Vladimir Zherebchevsky, Grigory Feofilov, Tatiana Lazareva, Alina Rakhmatullina, Nikolay Maltsev, Nikita Prokofiev
on behalf of the ALICE collaboration

Saint-Petersburg State University

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# Outline

- ALICE Inner Tracking System: upgrade strategy
- ALICE Pixel Detectors
- Study of the characteristics of ALICE pixel detectors
- Summary and next plans

# ALICE Inner Tracking System: upgrade strategy

90 Outer layer Staves (1500mm)

54 Middle layer Staves (900mm)

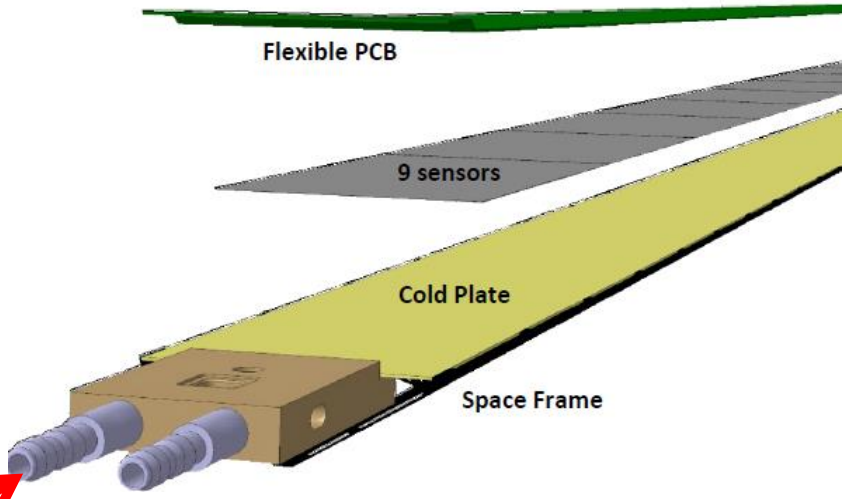
48 Inner layer Staves

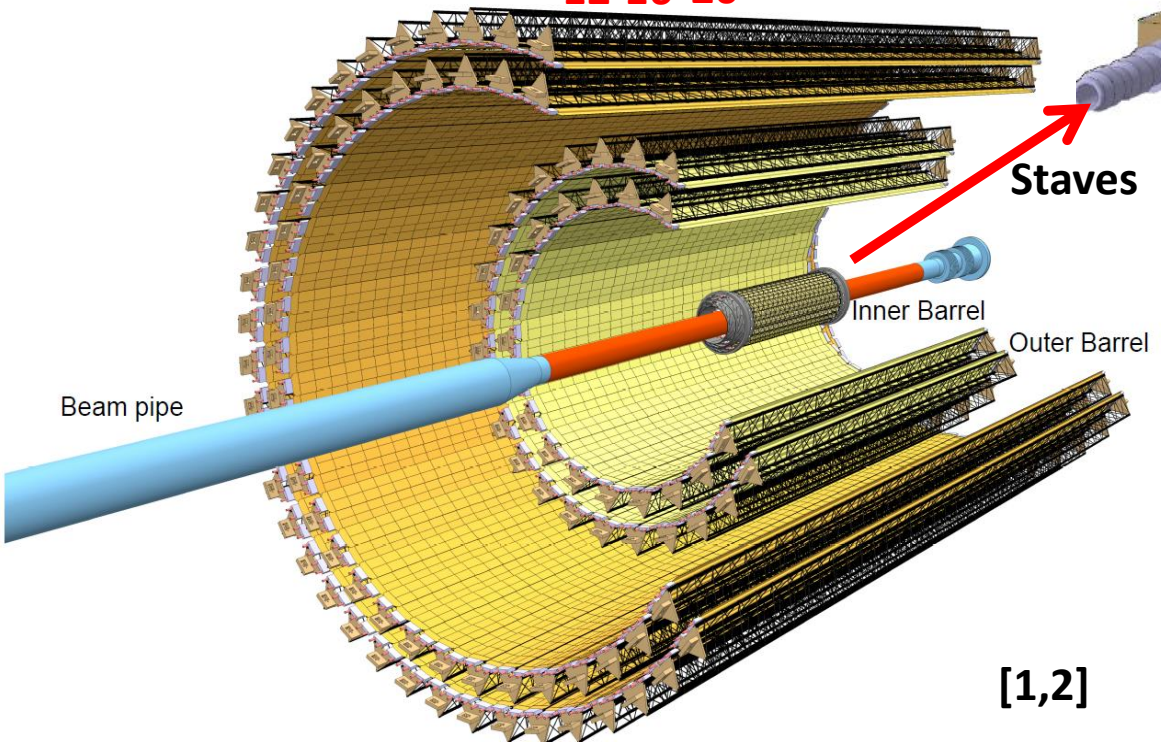
290mm

48 42 30 24 12 16 20

The main goal is to investigate particles with heavy flavors.

## Inner Barrel Stave




Staves

Stave :

1. Hybrid Integrated Circuit (HIC)
2. Cold plate
3. Space frame

[1,2]

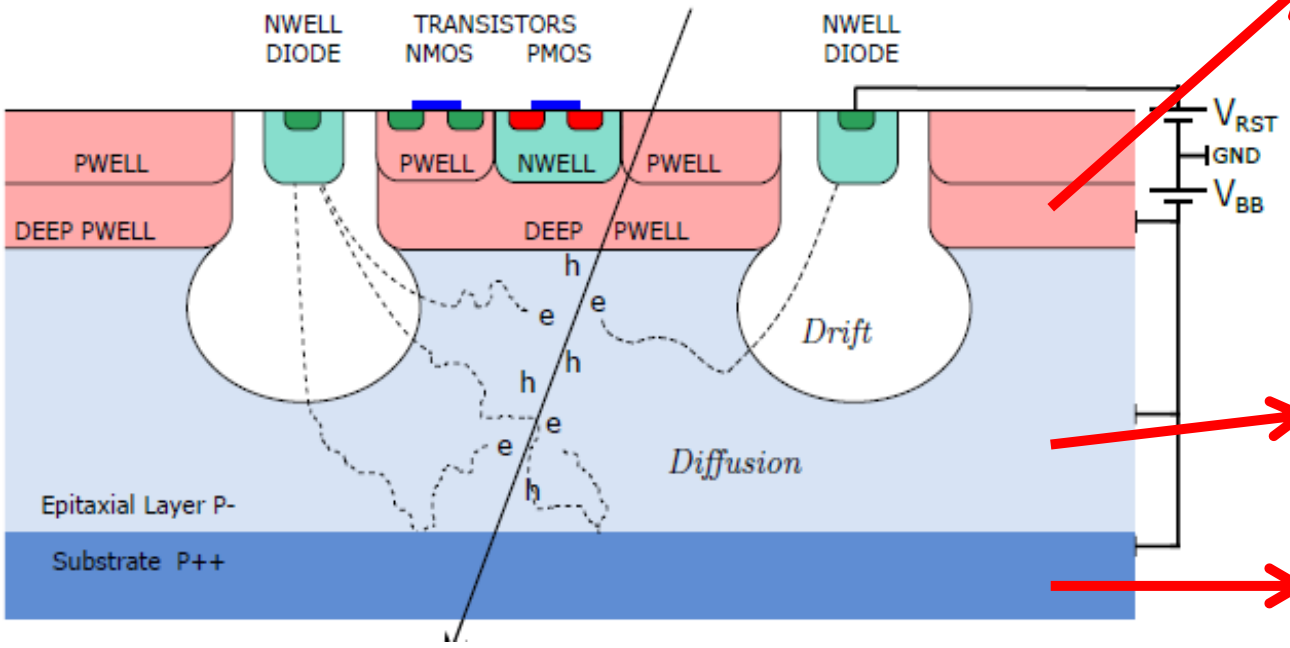
Barrel: 7 layers of Monolithic Active Pixel Sensors (MAPS)

$1.25 \cdot 10^{10}$ pixels

~$10 m^2$ total active area

# ALICE Pixel Detectors (ALPIDE)

## ALPIDE using TowerJazz 180nm CMOS Imaging Process




[3]

Shielding the other NWELLs different from the collection electrode, preventing them from collecting signal charge which then would be lost for readout. Full CMOS within the pixel

High resistivity(> 1kΩ ·cm) p-type epitaxial layer (25µm)

Low-resistivity p-type substrate

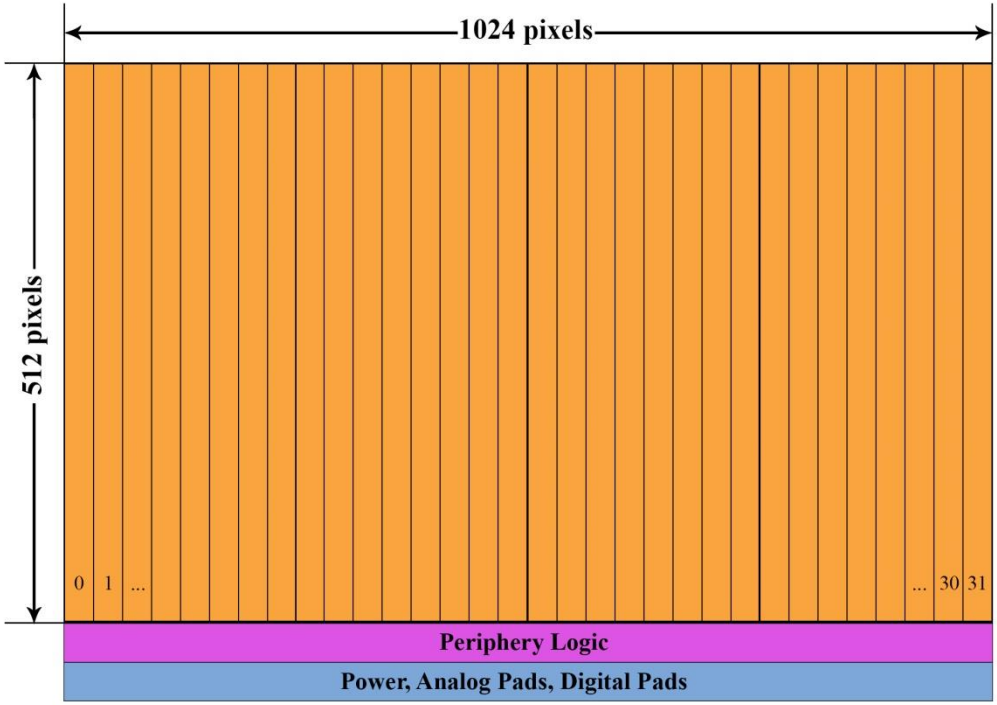
Small n-well diode (2-3 µm diameter), ~100 times smaller than pixel →low capacitance [4]

The gate oxide thickness of 3 nm → robustness to Total Ionizing Dose

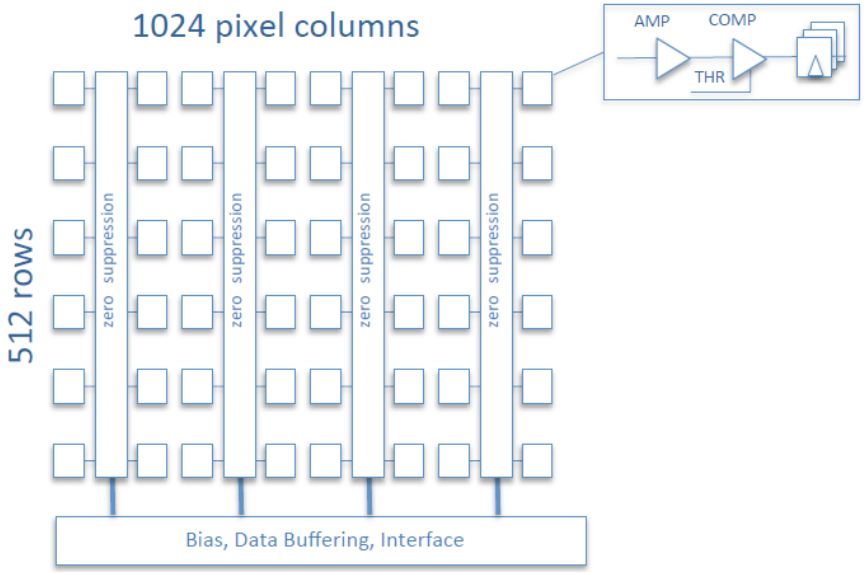
Possibility to apply back bias to the substrate can be used to increase depletion zone around NWELL collection diode: S/N ratio increases, higher efficiency

# ALICE Pixel Detectors (ALPIDE)

## Pixel matrix of ALPIDE




[2]




**The pixel matrix is divided into 32 regions.**

30 mm

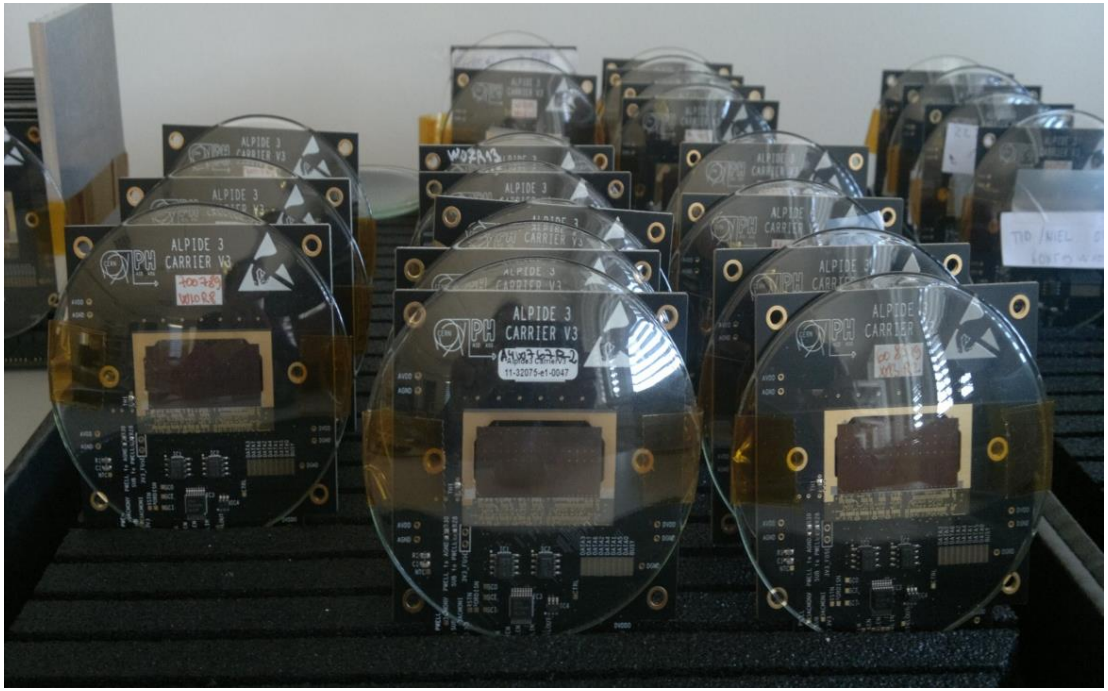
15 mm

**In the space between each pair of double columns is a priority encoder circuit that performs the asynchronous reading of a signal from the pixels in these columns.**

**The edge of the detector also presents Periphery logic, Analog and Digital pads and Power circuits.**

# Study of the characteristics of ALICE pixel detectors

**In this report: investigations of two irradiated and one non-irradiated detectors at different temperatures.**




ALICE pixel detectors – ALPIDE (final version) **[5]**

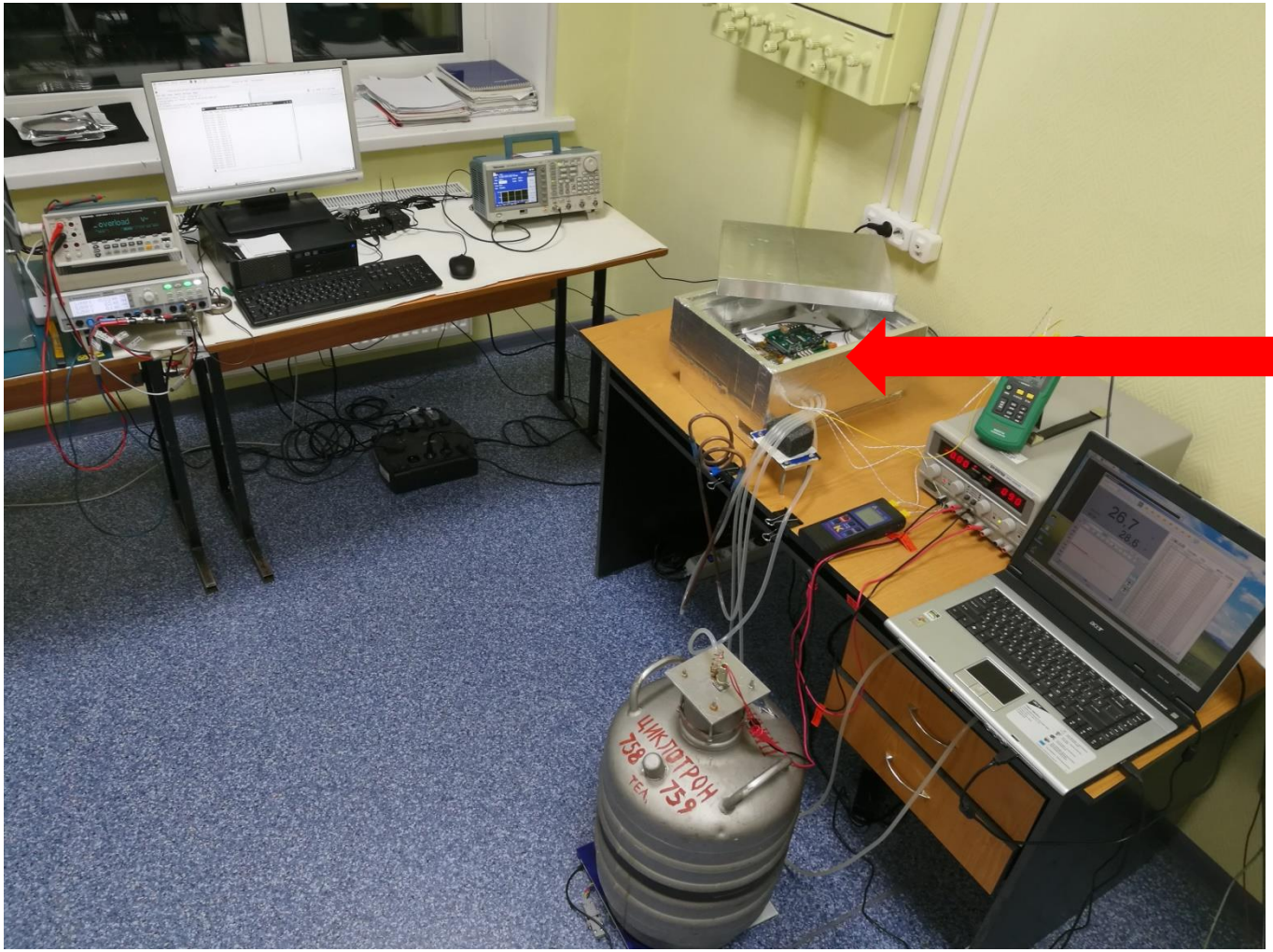
**Detectors were irradiated with X-rays with $V_{bb}$ = -3V applied**

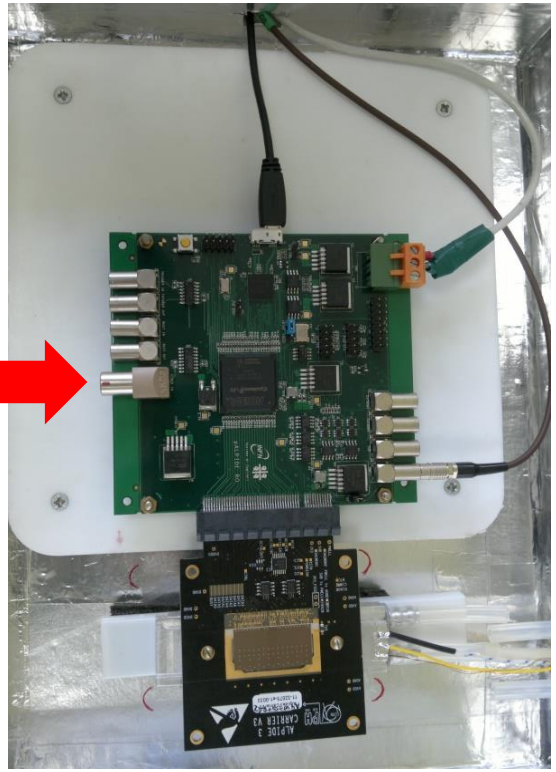
**Chip W8R22 – 60 krad (low dose)**

**Chip W7R12 – 300 krad (high dose)**

# Study of the characteristics of ALICE pixel detectors:

## Experimental setup with a cryogenic module.

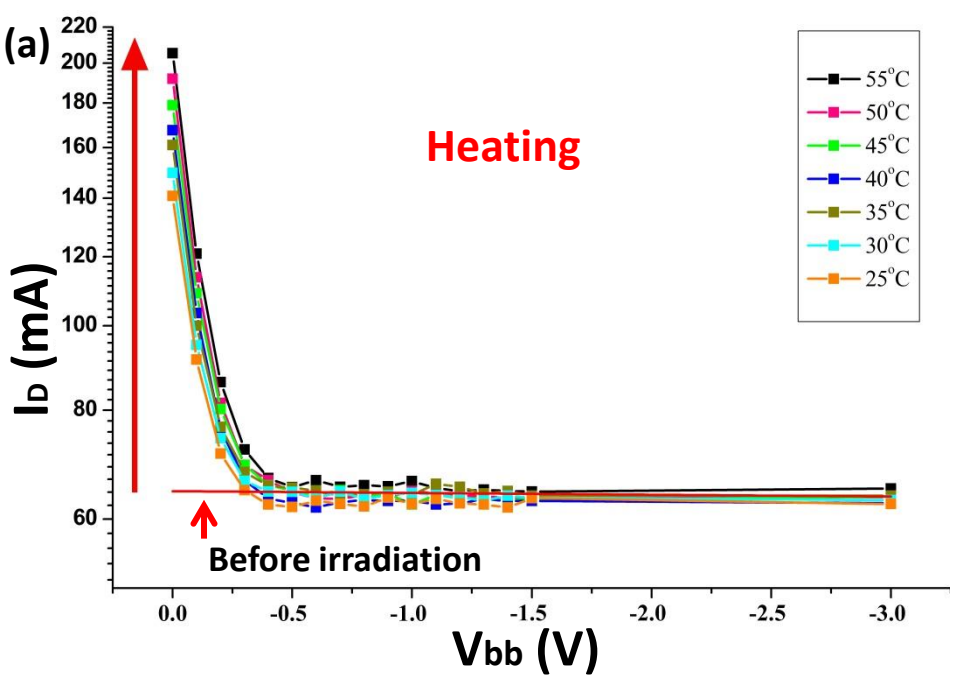


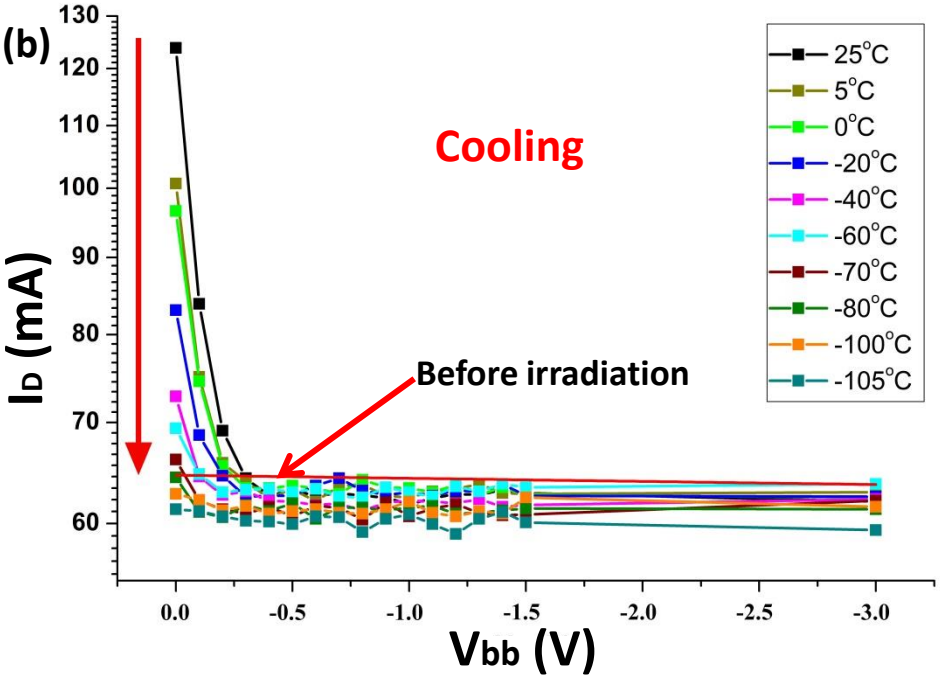



**Allows us to cool the detectors down to -120$^{o}$C and to heat them up to +60$^{o}$C.**

# Study of the characteristics of ALICE pixel detectors:

## the current of the detector digital part vs. back bias voltage ($V_{bb}$).




1. After irradiation with high dose the current increased;

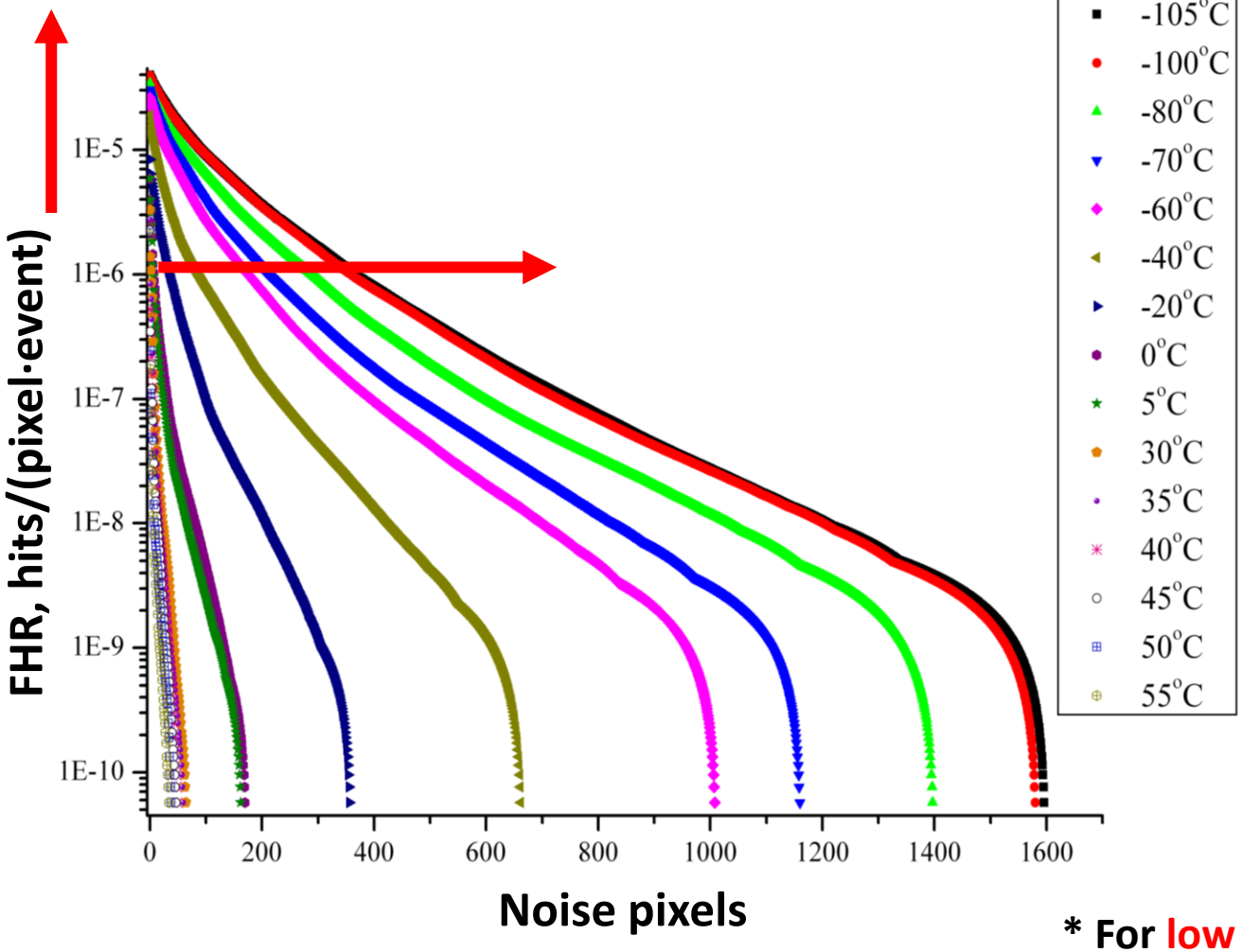
2. With increasing temperature the current increases;

3. With decreasing temperature, the current decreases. Starting at a temperature -60 °C, for irradiated (high dose) chip the digital current at $V_{bb}$ = 0 V has the same values as before irradiation.

Chip W7R12 – 300 krad (high dose), detector was irradiated at $V_{bb}$ = -3V.

# Study of the characteristics of ALICE pixel detectors:

## results of noise test.




$$FHR = \frac{\text{number of hits}}{\text{number of pixels} \cdot \text{number of events}}.$$

**Chip W7R12 – 300 krad (high dose):**

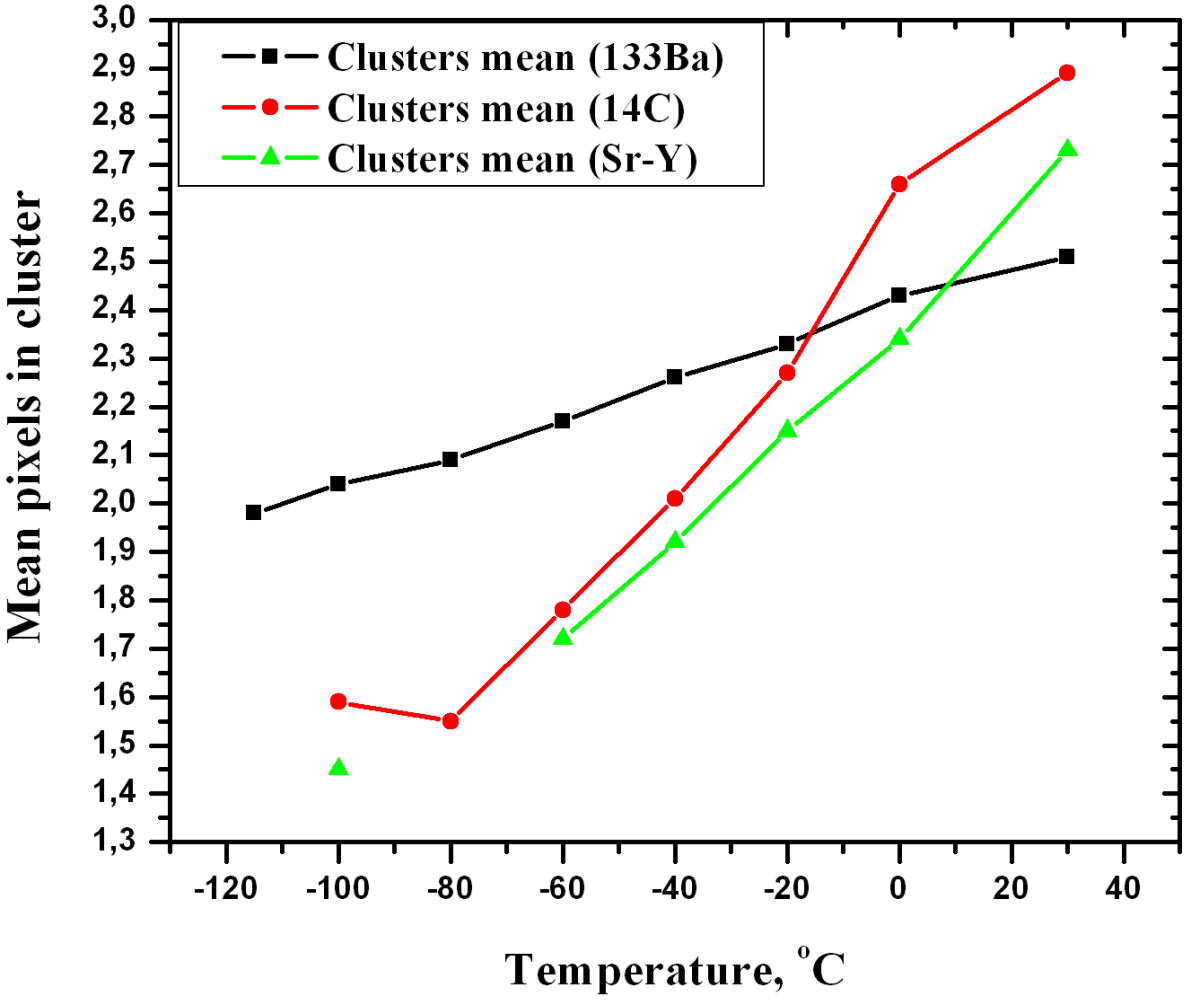
**1. The number of noisy pixels to be masked to achieve certain fake-hit rate increases with the lowering of temperature**

**2. Fake-Hit Rate (FHR) also increases with decreasing temperature**

*** For low dose irradiated chip and non-irradiated chip fake-hit rate DID NOT change over the full temperature range: from -105 °C to +30°C**

# Study of the characteristics of ALICE pixel detectors:

## results of cluster analysis (size of cluster vs. temperature).




**Pixels are located close to each other → the charge is shared by neighbouring pixels → clusters appear**

Sources used:

| Source | Energy, keV | Rad. type |
|---|---|---|
| $^{133}Ba$ | 5.64 | γ |
| $^{14}C$ | cont. spect. | β |
| $Sr-Y$ | cont. spect. | β |

**[5]**

**Average cluster size does not exceed 3 pixels. A decrease in temperature leads to a decrease in cluster size.**

**Chip W7R12 – 300 krad (high dose)**

# Summary

- The cryogenic module was constructed for investigations of the characteristics of the irradiated ALICE pixel detectors. The investigations of characteristics of some samples of irradiated ALPIDE sensors were carried out at temperatures from +55$^{o}$C to -105$^{o}$C;

- The detectors meet the requirements of the ALICE collaboration [1] in terms of noise and FHR and this type of sensors is being used in the ongoing upgrade of the Internal Tracking System. The ALICE upgrade preparations are well on-track for new physics studies after 2020;

- Several effects of noise characteristics dependence on temperature, that were discovered in the given samples of irradiated detectors, are planned to be studied further including the performance of sensors at cryogenic temperatures that might be useful for future applications.

# Thank you for attention!

# Literature


1) The ALICE Collaboration. “Technical Design Report for the Upgrade of the ALICE Inner Tracking System”. In: J. Phys. G41 (2014), p. 087002.

2) L.Musa, ECFA High Luminosity LHC Experiments Workshop, Aix-Les Bains, 3-6 October 2016, https://indico.cern.ch/event/524795/timetable/

3) Felix Reidt CERN-THESIS-2016-033

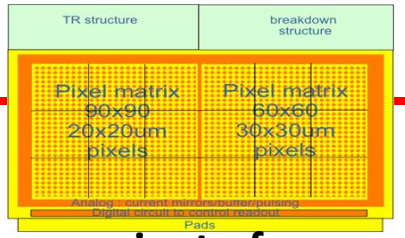
4) V.I. Zherebchevsky, et. al., «New pixel detectors for alice at lhc and for nica experiments», XXIV International Baldin Seminar On High Energy Physics Problems Dubna, September 17-22, 2018

5) V.I. Zherebchevsky, “ALPIDE at cryogenic temperatures”, ITS upgrade characterisation WP5 meeting at CERN, 4.10.2017, https://indico.cern.ch/event/670889/

6) M. Mager, “ALPIDE, the Monolithic Active Pixel Sensor for the ALICE ITSupgrade” Nuclear Instruments and Methods in Physics Research A 824 (2016) 434–438

# BACK-UP SLIDES

# ALICE Pixel Detectors (ALPIDE family)




2012 — **Explorer** → **Explorer-1,2**

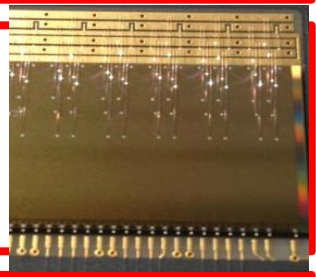
Two submatrices: 90x90 array of 20 x 20µm pixels and 60x60 array of 30x30µm pixels. Each sub matrices is divided in 9 sectors with one variant of collection electrode(analogue readout). Investigations: pixel geometry, starting material, sensitivity to radiation.

2013 — **pALPIDEss**

Matrix with 64 columns x 512 rows of 22µm x 22µm pixels. (in-pixel discrimination and buffering). Study priority encoder and the front-end electronics

May-2014 — **pALPIDE-1**

Full-scale prototype to study system effects: 1024 columns x 512 rows of 28µm x 28µm pixels. Four sectors with different pixels.



May-2015 — **pALPIDE-2**

Four sectors with different pixels. Optimization of several circuit blocks. Allows integration into ITS modules

Oct-2015 — **pALPIDE-3**

Eight sectors with different pixels. Final interfaces, more features including 1.2 Gbit/s output serial link.

Jul - 2016 — **ALPIDE – Final Version**

[4]

## ALICE Pixel Detectors (ALPIDE family)

## Pixel detector general requirements (from Technical Design Report for the Upgrade of the ALICE ITS)

| Parameter | Inner Barrel (IB) | Outer Barrel (OB) | ALPIDE Performance |
|---|---|---|---|
| Silicon thickness | 50 µm | 100 µm | |
| Chip dimension | 15 mm x 30 mm | 15 mm x 30 mm | |
| Spatial resolution | 5 µm | 10 µm | 5 µm (IB), 5 µm (OB) |
| Power density | < 300 mW/cm$^2$ | < 100 mW/cm$^2$ | 40 mW/cm$^2$ (IB), 30 mW/cm$^2$ (OB) |
| Max. integration time | 30 µs | 30 µs | 10 µs |
| Detection efficiency | >99% | >99% | >99% **Upper limit!** |
| Fake-hit rate | <$10^{-5}$(TDR),<$10^{-6}$* /event/pixel for IB and OB | | <<<$10^{-6}$ /event/pixel |
| Total Ionizing Dose | 270 krad<br>2.7 Mrad* | 10 krad,<br>100 krad* | Up to 500 krad |
| Non-Ionizing Energy Loss (1 MeV $n_{eq}$/cm$^2$) | 1.7 x $10^{12}$ (TDR),<br>1.7 x $10^{13}$* | 1.7 x $10^{11}$ (TDR),<br>1.7 x $10^{12}$* | Up to 1.7 x $10^{13}$ |

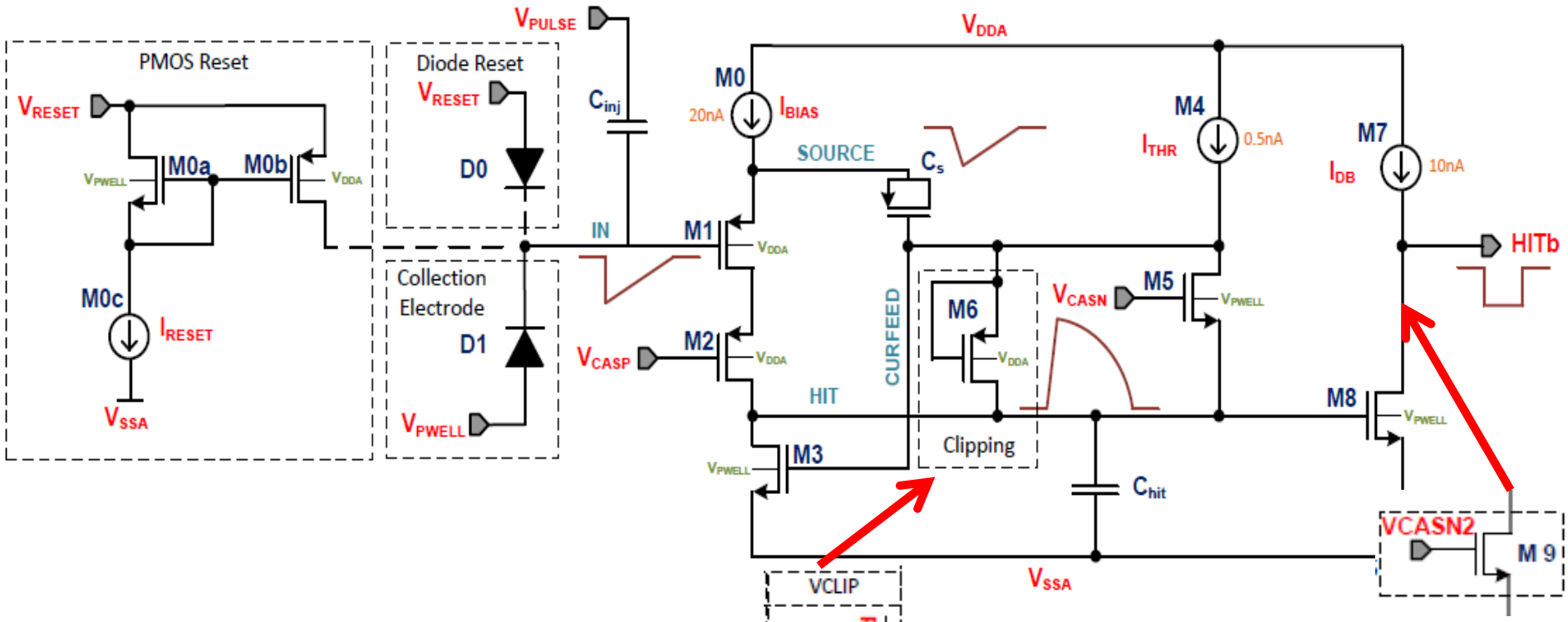
radiation load integrated over the approved program (~ 6 years of operation) **[1]**

*revised numbers with respect to ALICE TDR (factor 10)

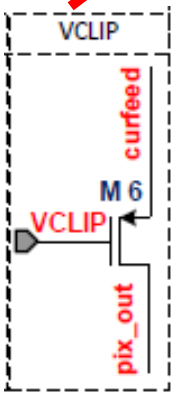
# Full-scale Pixel Detector prototypes (pALPIDE -1,2,3)

## A comprehensive scheme for the pixel front-end circuit
## Including all possible variations

### For pALPIDE-1,2




### For pALPIDE-3
### for sectors: 3,4,5,7
### add VCLIP



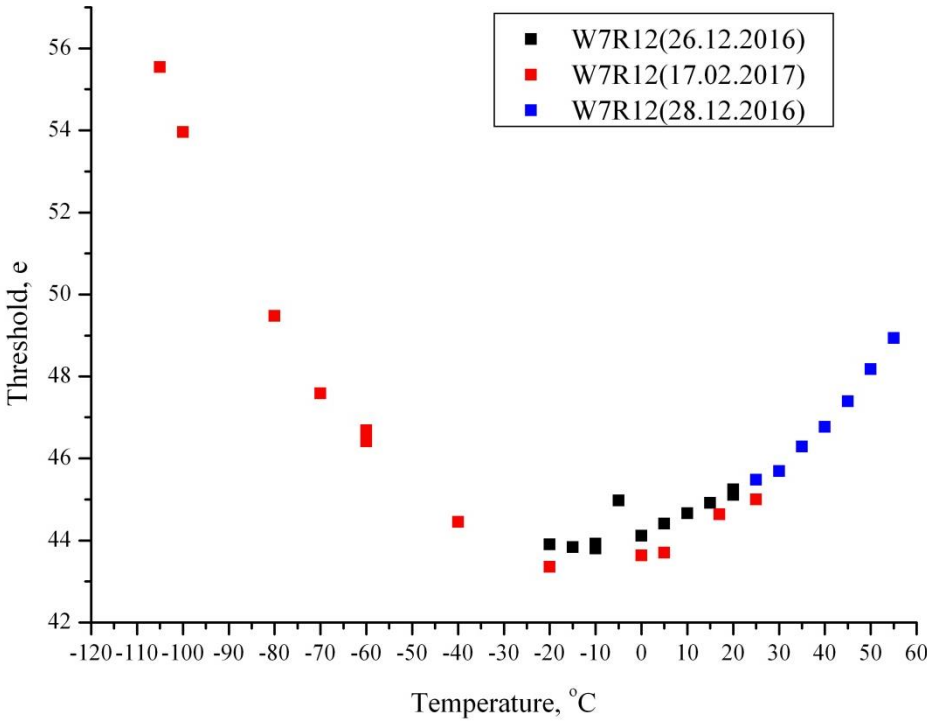

### For pALPIDE-3
### for sectors: 0,3,4,5,7
### add VCASN-2 (M9)

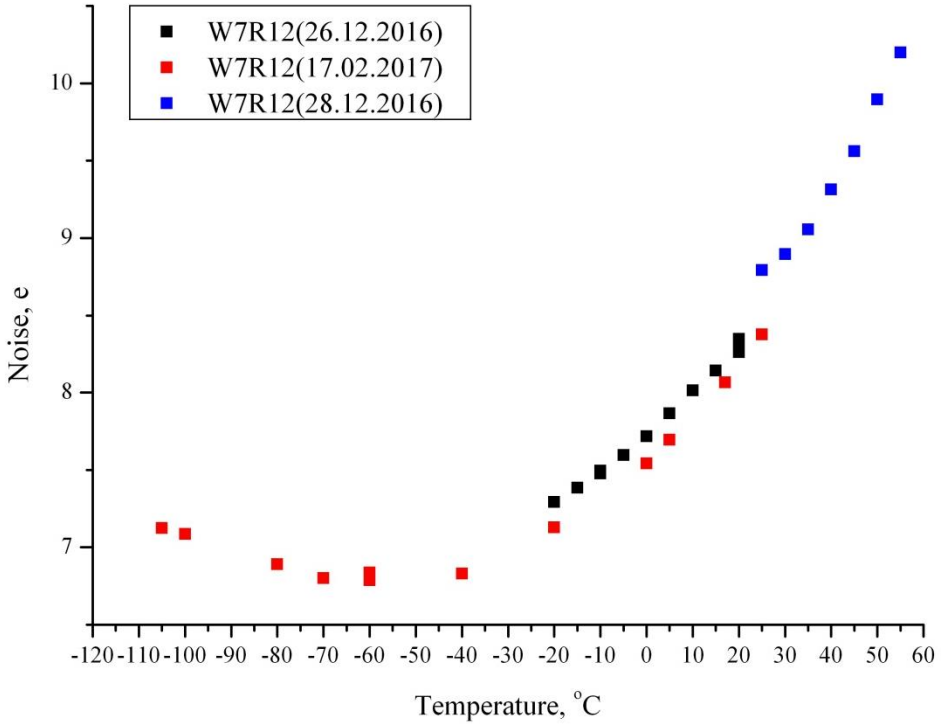
[6]

# Study of the characteristics of full-scale Pixel Detector prototypes

**Results for high dose irradiated chip** **Threshold Scan**

## Chip W7R12




**Before irradiation the threshold was ~ 85 e,**
**after irradiation (300 krad)**
**the threshold was ~ 45-50 e**

**Before irradiation the noise was ~ 6 e,**
**after irradiation (300 krad)**
**the noise was ~ 14 e**

**The threshold goes up both with increasing temperature and with lowering temperature, but initial value (before irradiation) of the threshold is not reached.**

**[4]**

# The ALPIDE characteristics studies

**Results for high dose irradiated chip**

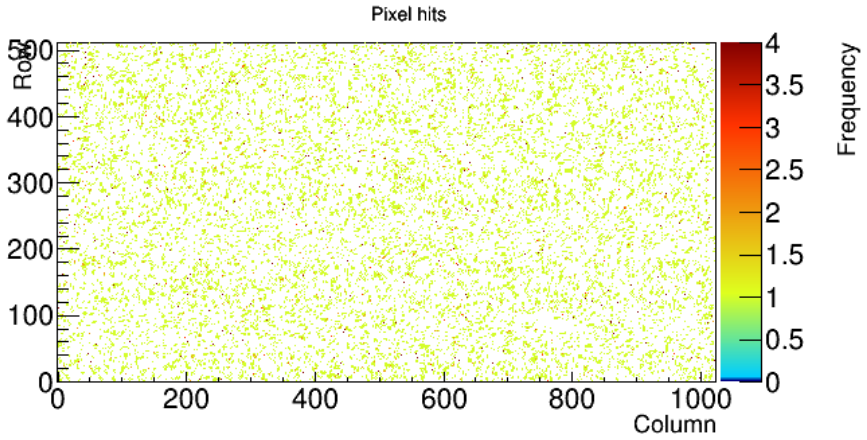
**Source test + Cluster analysis**

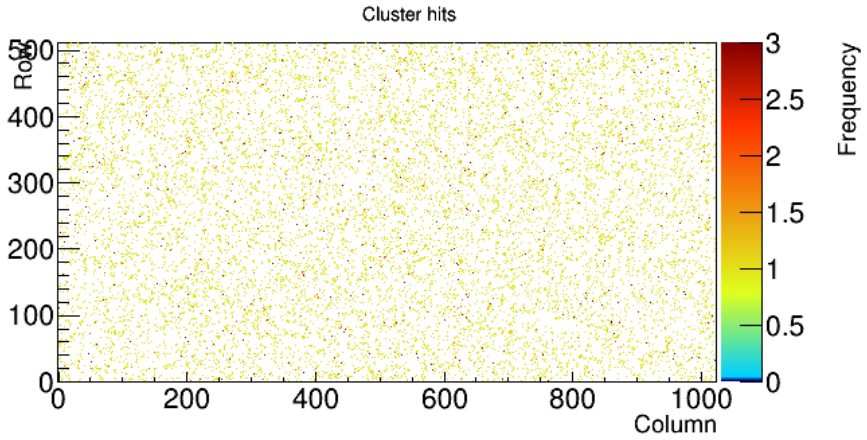
**Chip W7R12**

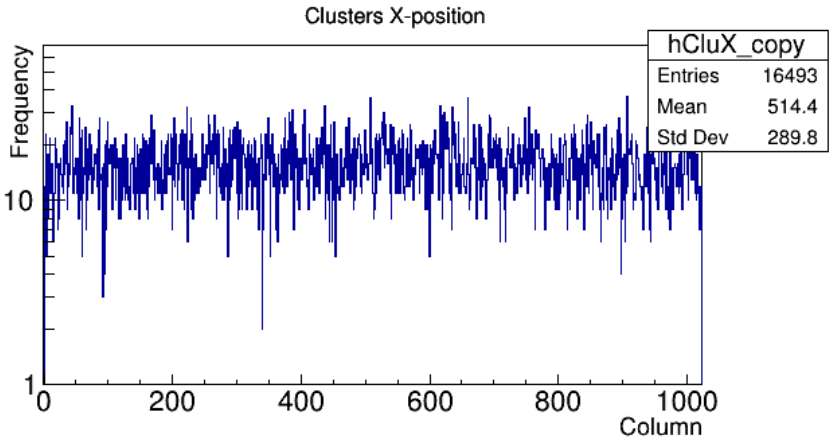
**Masked**

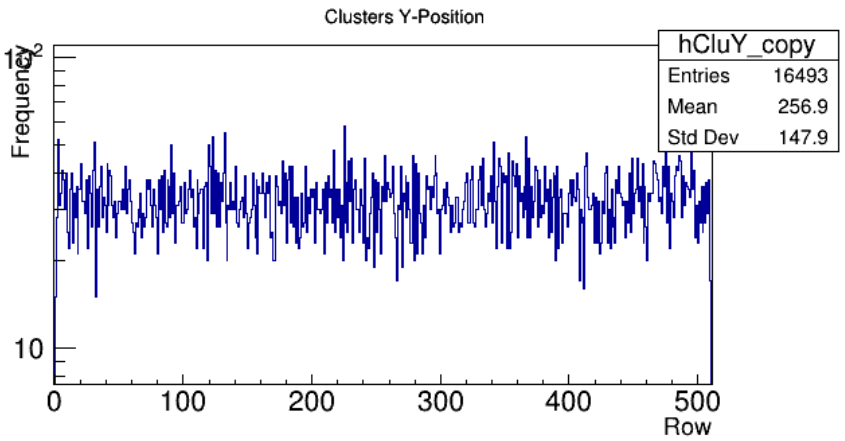
**Triggers: 2000000**

**Vbb = -3V**



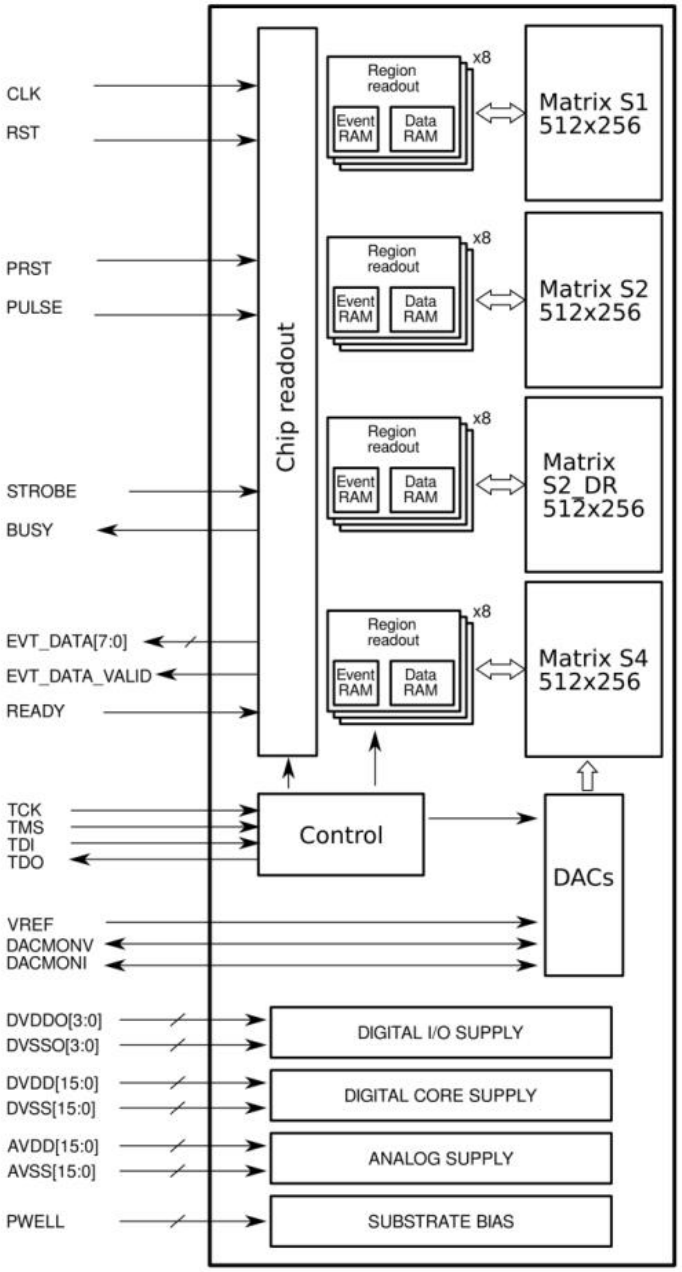




**Source: 133Ba, chip temperature -115 $^{o}$C**

**[4]**

# ALICE Pixel Detectors (ALPIDE family)




**A general block diagram of pALPIDE-1,2**

**All the analogue signals required by the front-ends are generated by a set of 11 (for pALPIDE-1,2) and 14 (pALPIDE-3) on-chip digital-to-analog converters (DACs).**

**The region readout units contain multi-event storage SRAM memories.**

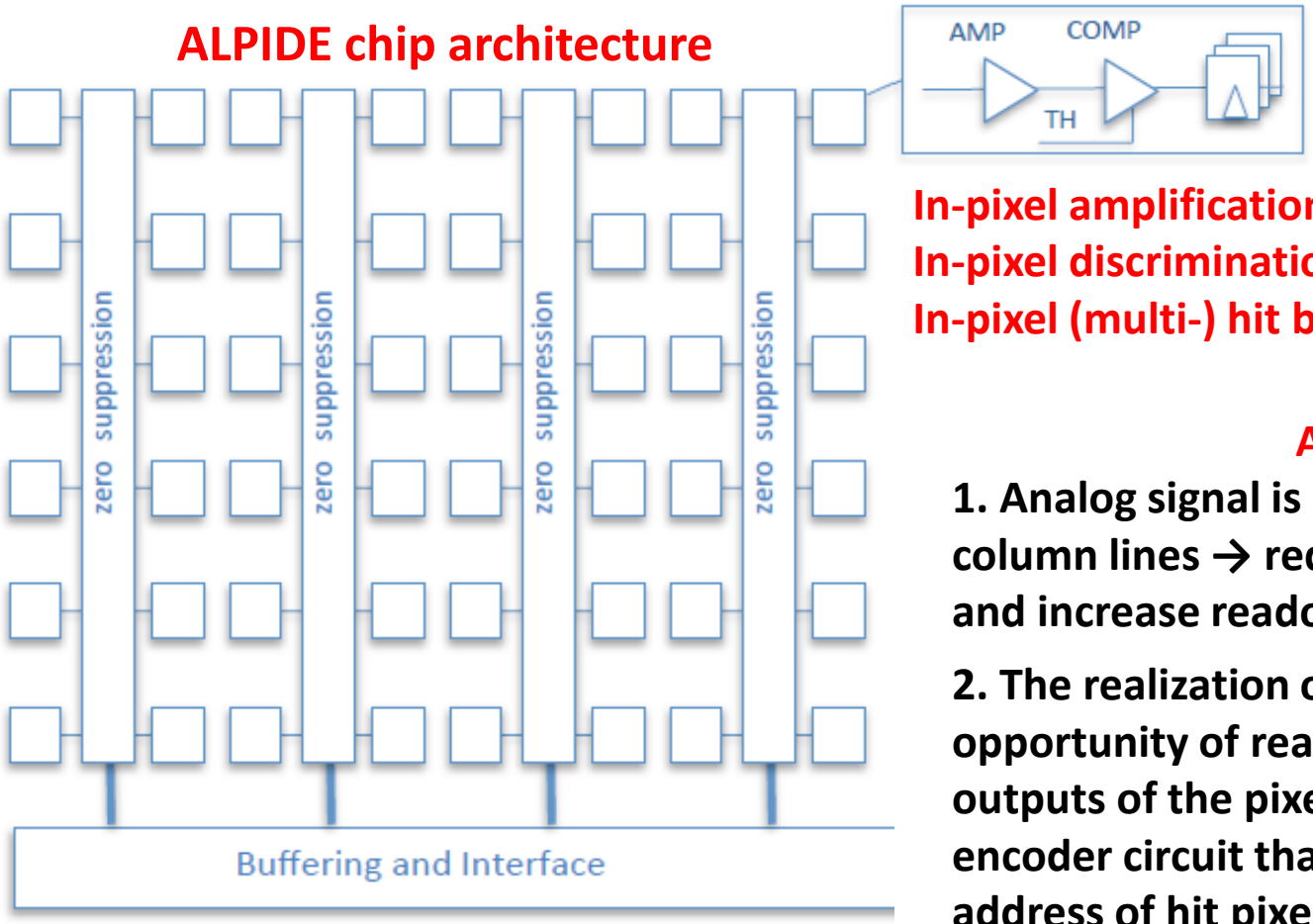
**Hit data from the 32 region readout blocks are combined and transmitted on a parallel 8-bit output data port.**

**A top-level Control block provides full access to the control and status registers of the chip.**

**[1]**

# ALICE Pixel Detectors (ALPIDE)

## ALPIDE chip architecture




**In-pixel amplification**
**In-pixel discrimination**
**In-pixel (multi-) hit buffer**

**The zero suppression is performed within the matrix. Address-Encoder Reset-Decoder circuit is employed. It can either be controlled by an external trigger signal or operated in continuous acquisition mode.**

### Advantages

**1. Analog signal is no longer driven over the column lines → reduce power consumption and increase readout speed.**

**2. The realization of in-pixel discriminators: opportunity of readout, in which the digital outputs of the pixels are scanned by an encoder circuit that directly produces the address of hit pixels as output.**

**3. The circuit works in a way that the pixel hit register is reset after the read operation and the circuit will move on to the next hit pixel to encode its address. The procedure is iterated until the full pixel matrix is read out.**

[2]