ASIC EVOLUTION FOR PARTICLE PHYSICS AND ASTROPHYSICS

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Abstract

- Construction of the advanced megascience facilities, basing on advanced particle detector technologies, is closely connected with development of read-out electronics, having as a core element – Application Specific Integrated Circuit (**ASIC**)
- In order to reach limit specifications of multichannel detector setups a whole set of factors defines ASIC design. The chips should provide new level of functionality, fitting to a **new set of constraints and trade-offs** on technical specifications (like an integration scale, power consumption, speed, radiation hardness) as well as economic- and technology-related ones
- The talk presents overview of the state of the art and evolution in ASIC design for particle physics and astrophysics

Aim is to present:

- Trends in ASIC design:
  history, state-of-the-art & what`s next
- Transistor scaling
- Example projects of ASICs
- Conclusions & References

Some main features of old ASICs (incl. LHC era)

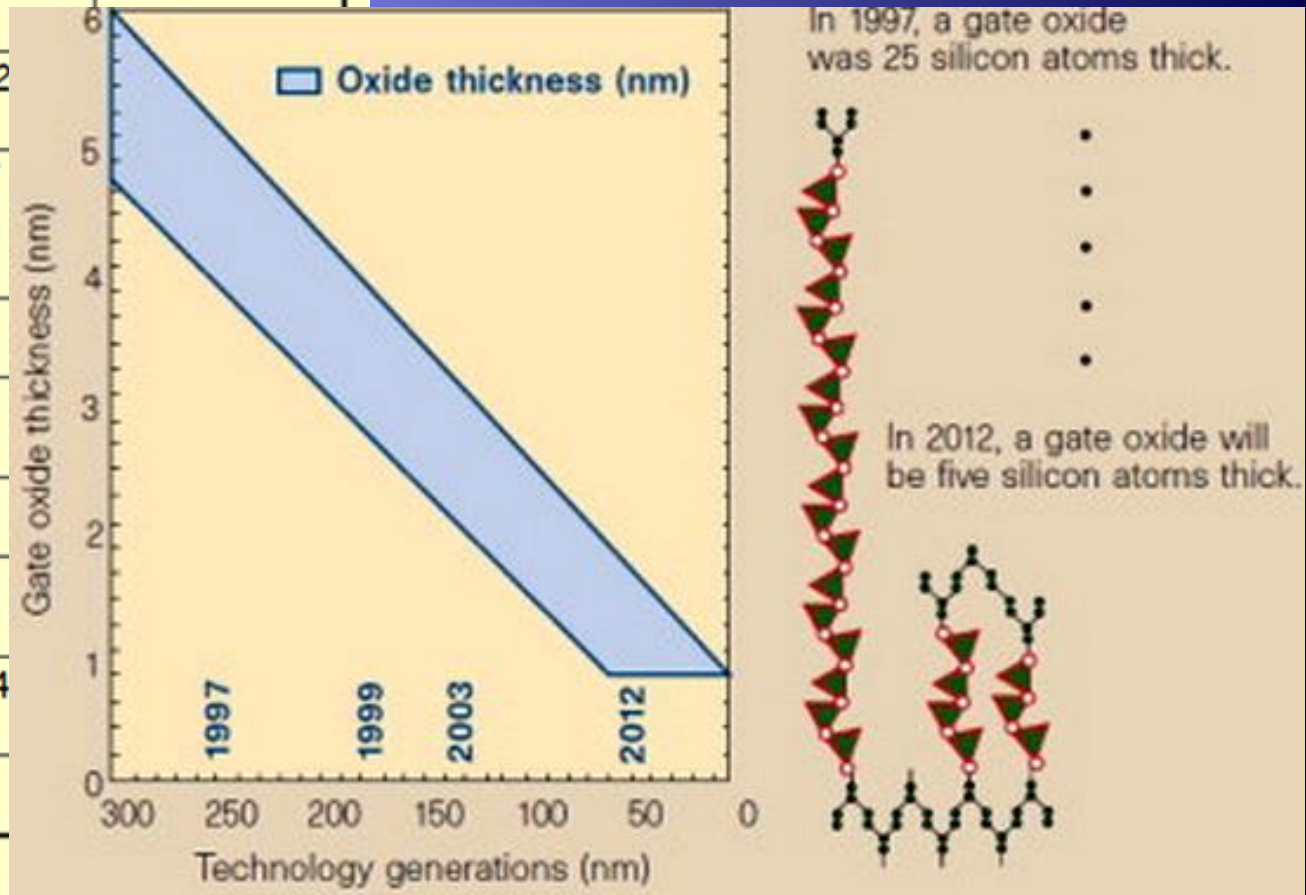
- Many different Bipolar, Bi-CMOS and CMOS processes in the range of 350.. ..250..130 nm from different foundries. No standardization at usage of both processes and design tools. Many different design teams with own strategy
- Integration scale for ASICs (typ.) – 8-32 channels per chip, area of 1 sq.sm. max, no ADC in FEE, separate chips for analog and digital parts
- Rad-hard TID level up to few Mrads. Provided by both process and RHBD hardening
- Power consumption – tens mW per channel
- 3-4 respins of prototyping before engineering run

Transistor scaling

ITRS Roadmap

	2004	2007	2010	2013	2016
Technology Node [nm]	90	65	45	32	22
Transistor count [Mtr]			1500	3092	
Transistor Density [Mtr/cm2]	77	154	309	617	
Chip Size	140				
Clock freq [GHz]	3		15		
Vdd	1.2	1.1	1.0	0.9	
DRAM half pitch	90	65	54	32	
Signal IO Pads	512	1024	1024	1024	
Power Pads	1024				

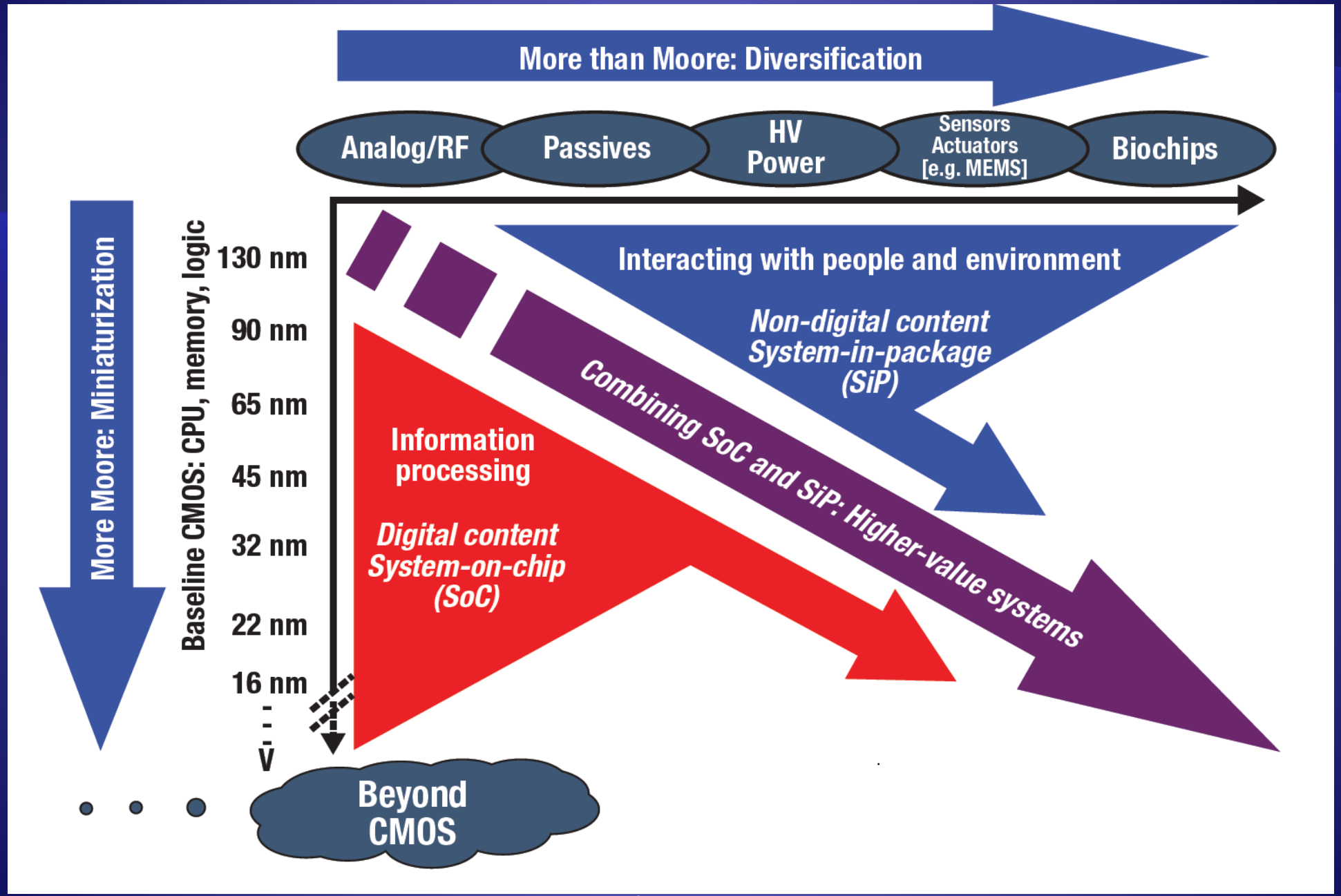
International Technology Roadmap for Semiconductors



How could near future ASIC looks like? (1 of 3)

- Ideally based on hybrid technologies (at element, chip, package, board and finally system levels, incl. data transfer) to effectively reach a limit functionality
- System level efforts should take over the element level design. The accent at design is done at system (architectural) questions → **SOCs** (systems on a chip) dictate a **mixed-signal** character of design route
- The demanded number of ASIC wafers is small and can't interest a manufacturer (10^6 channels at ~100 chs/chip and ~1000 chips/wafer→ **~10 wafers** only)
- Adaptation perspective ASIC for different projects as criterion of economic efficiency

More than Moore

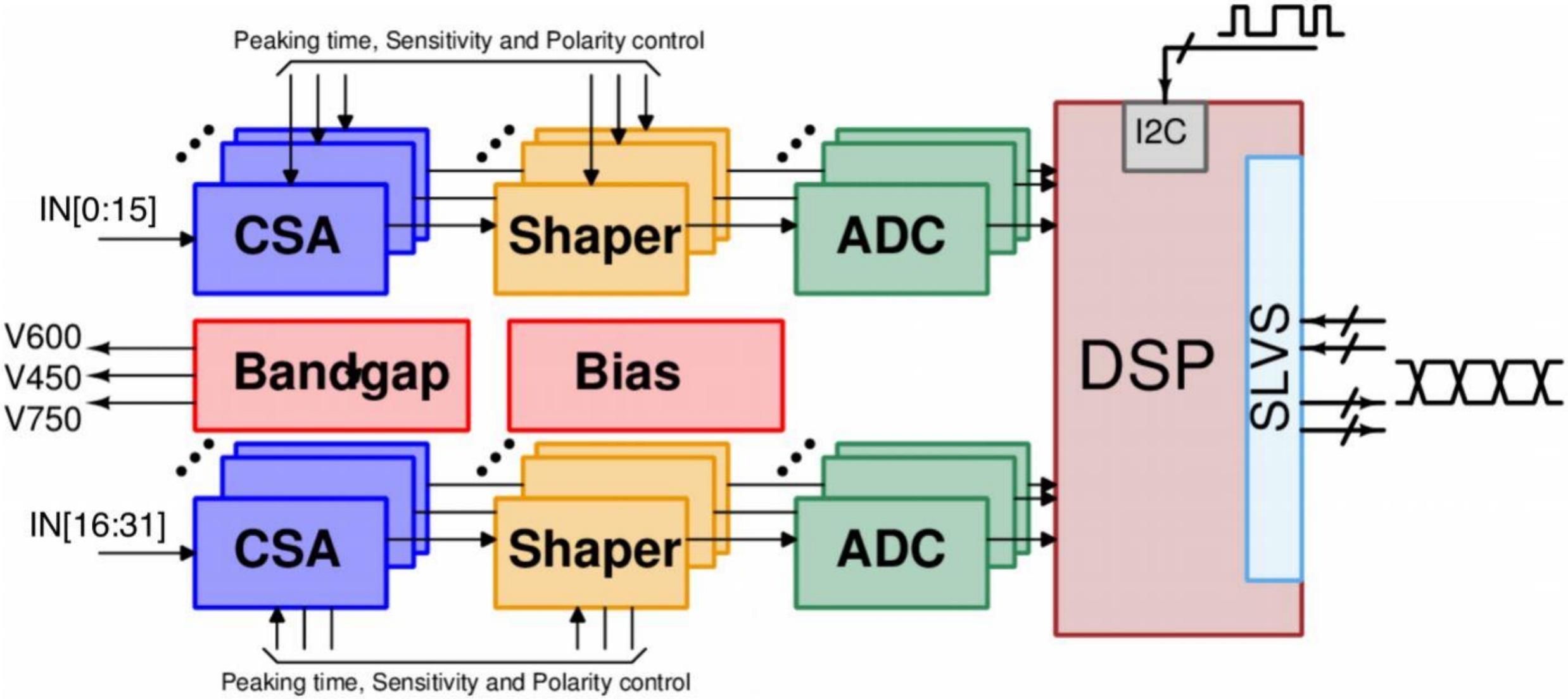


International technology roadmap for semiconductors , 2012 Update Overview

How could near future ASIC looks like? (2 of 3)

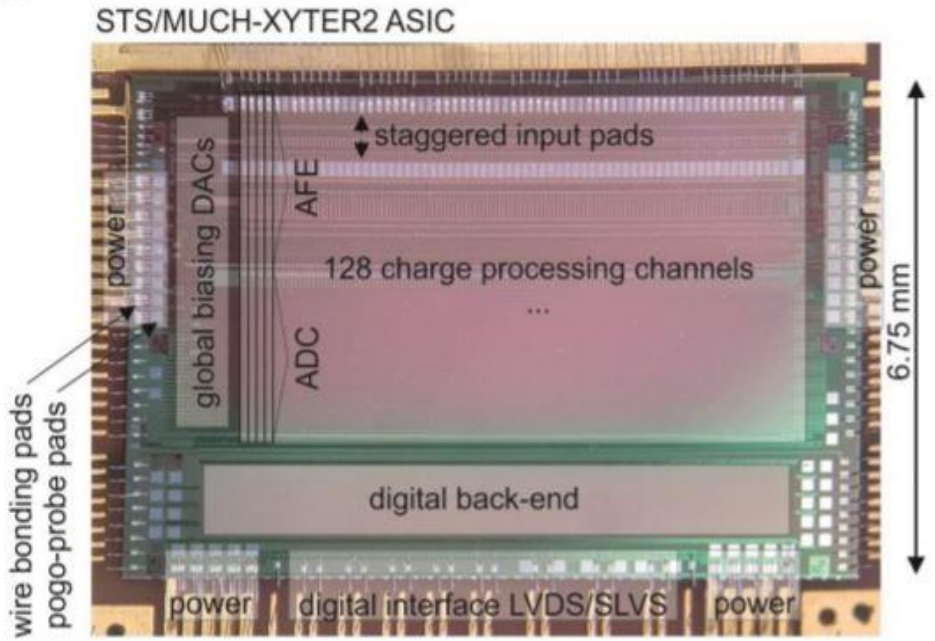
- Standardization in use of both pure CMOS technology processes (**180-130 nm for Analog** part and **65 nm for Digital** one) and community shared re-usable building block libraries
- Integration scale for ASICs (typ.) – **32-128** channels per chip, **built-in FEE ADC**
- Highly integrated very sensitive analog (where possible differential) front-end
- **Digitization** (8-10 bit resolution typ.) **at earliest stage** at less than 1V power supply headroom
- **Signal processing** mostly in digital domain (**DSP**)

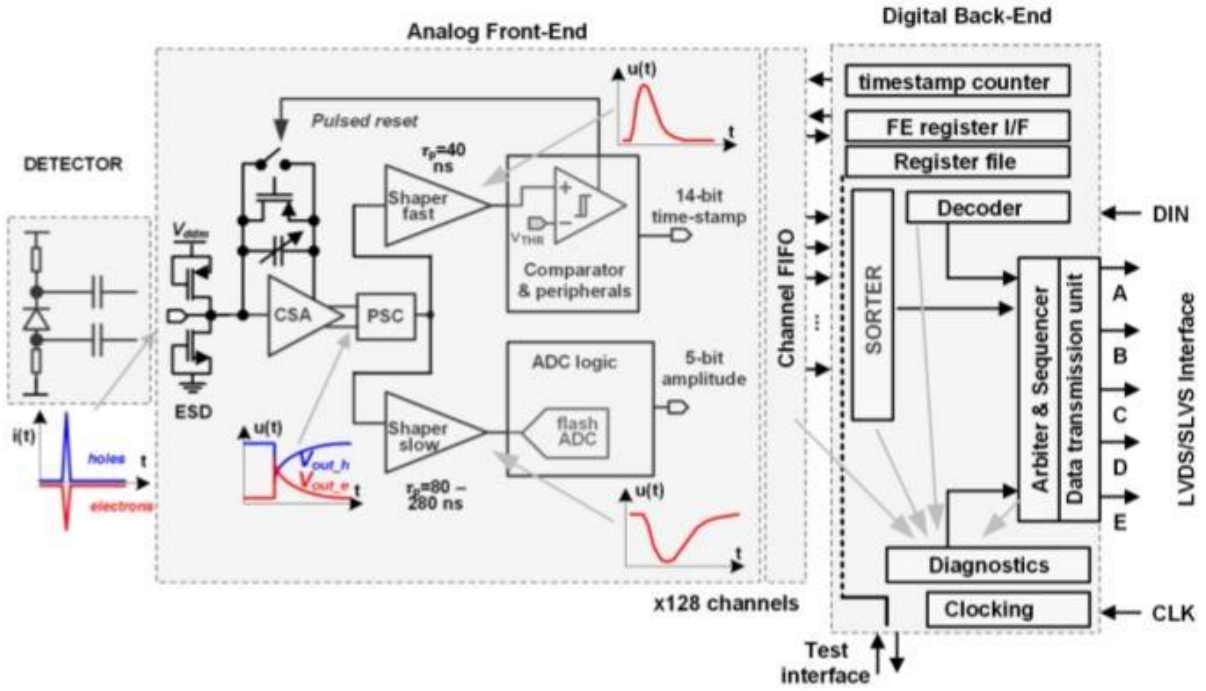
Example ASIC 1 – SAMPA (ALICE project)



Example ASIC 2 (CBM project)

AGH





128 channels + 2 test channels

charge sensitive amplifier (continuous+pulsed reset, switchable gains (STS/MUCH) + trim)

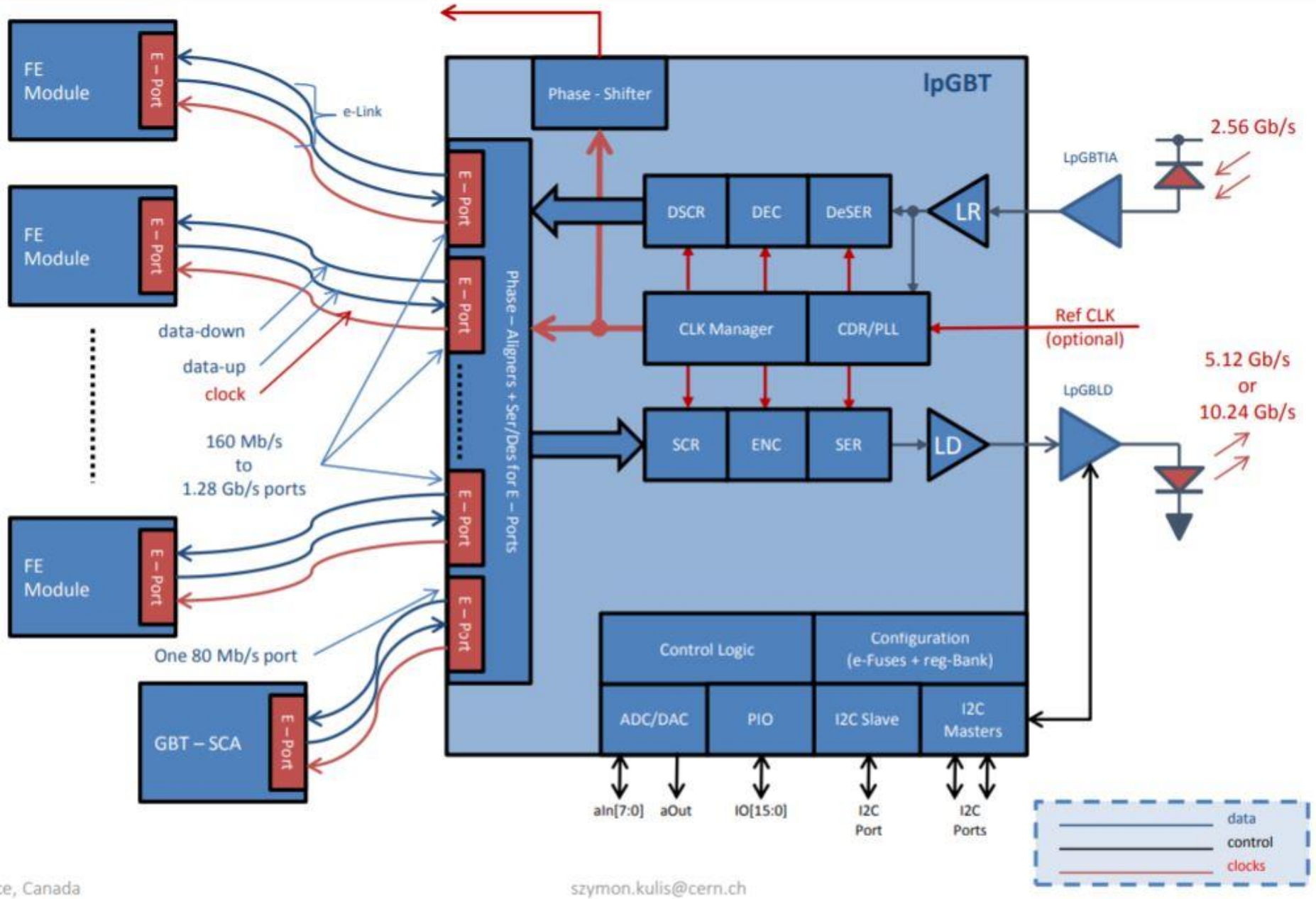
5-bit amplitude measurement (shaper slow + ADC)

14-bit timestamp measurement (shaper fast + leading edge discriminator)

How could near future ASIC looks like? (3 of 3)

- **High data rates** via output (preferably optical) serial interfaces with speed in multi-Gbps range (10 Gbps under design)
- **Big data processing** (for ex. CMS detector raw data >1000 Pbyte/day (1 Mbyte x 40 MHz)) starting **on detector**
- Chips will not be cheaper than before
- Very **difficult environment** on TID (up to 100 Mrad) and high magnetic field (ex. few Tesla)

lpGBT: High Speed SerDes



Example ASIC 3
(common project at CERN)

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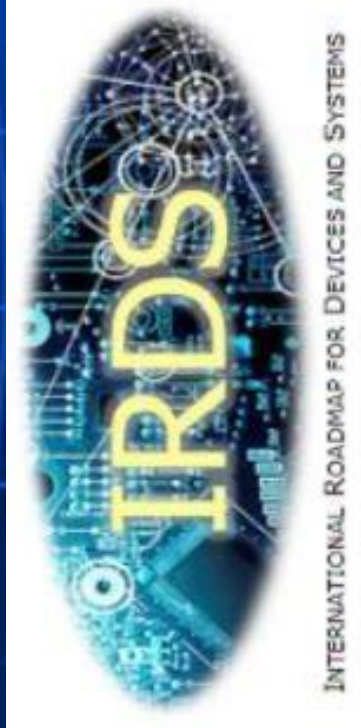
The Different Ages of Scaling
(Different methods for different times)

P.Gargini

1. Geometrical Scaling (1975-2002)
   1. Reduction of horizontal and vertical physical dimensions in conjunction with improved performance of planar transistors
2. Equivalent Scaling (2003~2024)
   1. Reduction of only horizontal dimensions in conjunction with introduction of new materials and new physical effects. New vertical structures replace the planar transistor
3. 3D Power Scaling (2025~2040)
   1. Transition to complete vertical device structures. Heterogeneous integration in conjunction with reduced power consumption become the technology drivers



Conclusions

ASICs are of the key elements of future of detector setups due to new challenges in integration scale

Available commercial **processes** today are well ahead of most requirements (including radiation hardness) foreseen for particle and astrophysics` installations

Today an optimum choice of CMOS technology node (in terms of functionality over cost) is between **130-180 nm for analog** designs to **65 nm for digital** ones

Almost all ASICs are **mixed-signal** ones

The solution of **system** (architectural, structural) problems will demand substantially higher efforts to create not separate components, but whole systems on chip (**SoC**)

Conclusions (2)

The **"Rad-hard by design"** approach for commercial CMOS technology is considered to be the best way of providing an **acceptable** radiation tolerance by circuital and layout techniques.

For radiation tolerance and temperature stability of the chips it is important to refine the existing libraries and design routes

The necessity of **much stronger collaboration** and coordination between all participants, sharing: the process of preparing human resources; the cost of expensive CAD and chip prototyping as well as steady updating design competences

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