

Design flow of the electronic units of multichannel detector systems for large physical experiments

Monday, 22 October 2018 15:40 (150)

The conducting of physical experiments at large accelerator facilities, of the FAIR (Germany) type requires the provision of readout and processing of signals from a large number of detectors. To solve these tasks there are used complicated electronic units, which are designed as application specific integrated circuits (ASIC). The design process is subject to hard requirements, bound with reading out a great number of detector signals, high frequency of signal emergence, diversity of data types, necessary for analysing the results of experiment. The report presents the description of a mixed ASIC design flow with account of the requirements of large physical experiments. The given flow permits to reduce design time, to increase reliability and optimise the ASIC architecture. Probation of the flow was executed in the course of designing IC prototypes for the 180 and 65 nm technologies, executing the functions of data processing and readout.

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Session Classification : Poster session and coffee-buffet

Track Classification : Facilities and advanced detector technologies