# Development of ASICs for experiments at NICA

*E. Atkin*
*for ASIC Lab of NRNU MEPHI*

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# Design Team

Eduard Atkin

Pavel Ivanov,

Dmitry Normanov

Artur Serazetdinov

Vitaly Shumikhin

Salavat Yamaliev

(NRNU MEPHI) in collaboration with:

Evgeny Usenko (INR RAS)

Alexander Solin (INP BSU)

# Introduction

Application Specific Integrated Circuits (ASICs) are one of the key complex technologies available to designers of multichannel detectors. A whole number of factors makes ASICs essential to Particle Physics and Astrophysics experiments. The most important factors are: integration scale, low power dissipation, radiation tolerance

Another important aspect nowaday is formation of a big flow of generated data in the multichannel structure of the readout electronics and, as a consequence, the need to increase the processing speed

The presentation shows the current activity of NRNU MEPhI ASIC lab on chip design for experiments at NICA. These are: 1) front-end chip for RPC and 2) data concentrator chip for back-end electronics

# Outline

**Back-end project**

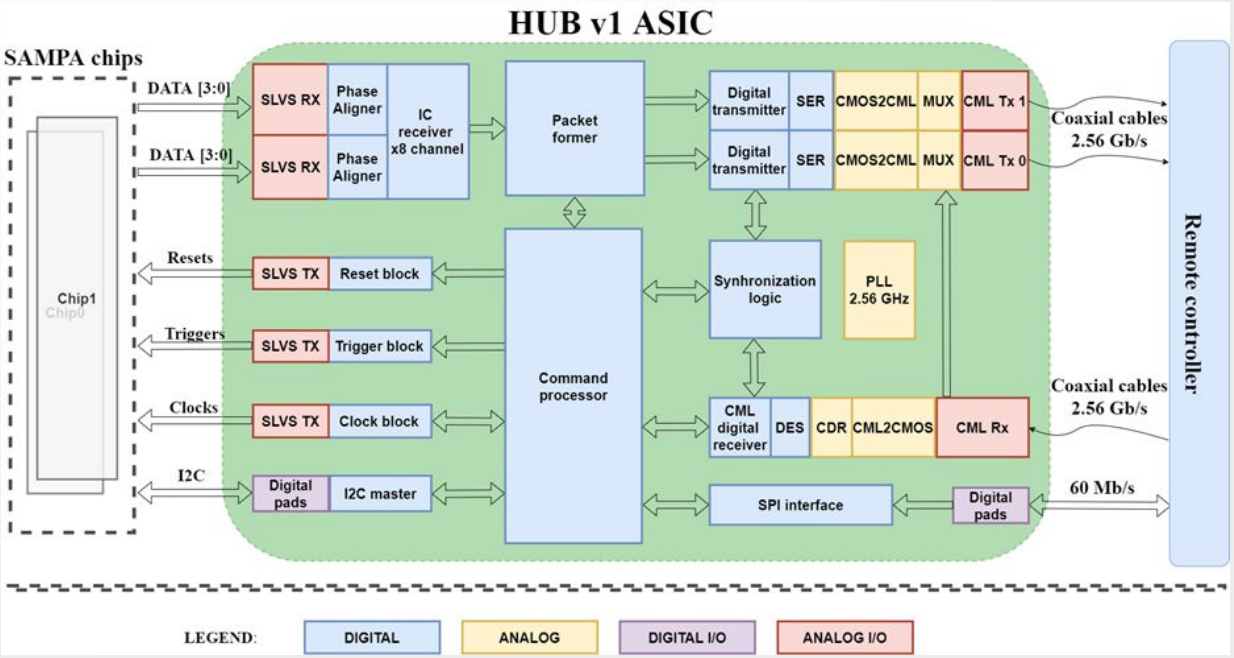
- ASIC Hub ver. 1: structure and specifications
- Test program (2 boards)
- Lab test bench
- The demonstrator concept
- The lab testbench in calibrated beam
- First results
- Hub chip status

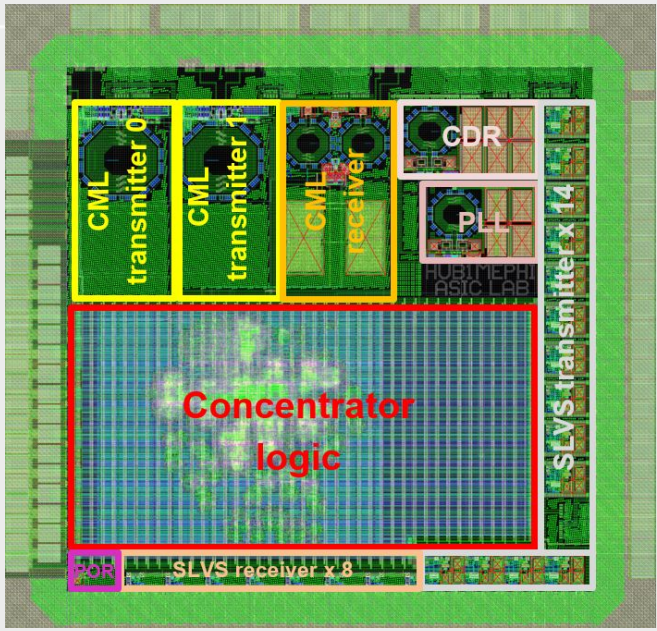
**Front-end project**

- Project review
- ASIC structure
- NINO channel structure (reference point)
- NINO channel structure (typical signals)
- Key goal characteristics

# ASIC Hub v1: structure and specs

main functions: data concentration from two SAMPA chips and their transfer to counting room via fast 2.56 Gb/s bi-directional interface




| Specifications | Value |
|---|---|
| Technology | TSMC CMOS 65 nm |
| I/O voltage | 2.5 V |
| Core voltage | 1.2 V |
| Power consumption | < 500 mW |

**1) Process – TSMC65 LP MS RF 1P9M_6X1Z1U_RDL;**
**2) Chip area – 1980 x 1980 um;**
**3) Bond pads – 111 (37 type CUP staggered & 74 type IN-LINE)**
**Pad size – 57 x 69 um**
**Pad Pitch – 60 um**
**4) Technological run of Nov. 2020**
**5) Samples – July 2021**
**2 types of packaging: CPGA 120 & caseless**

# Test program (2 boards)

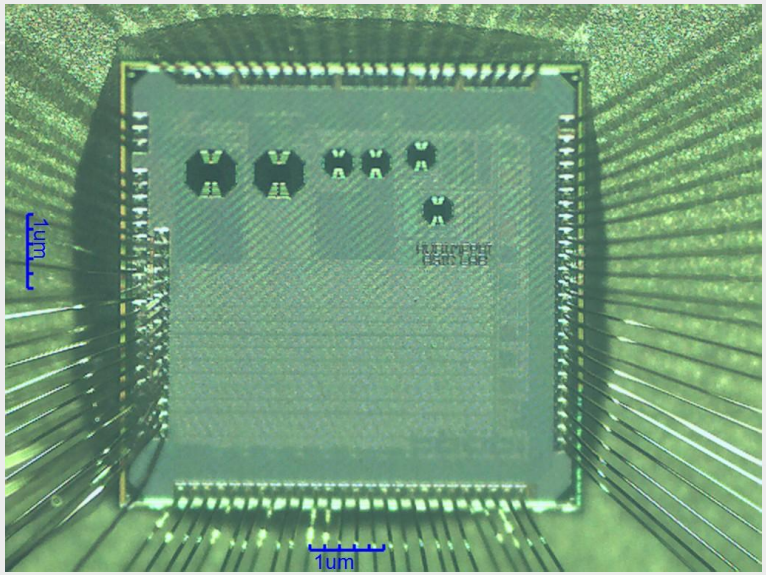
1) Laboratory phase (functionality & radiation tolerance)

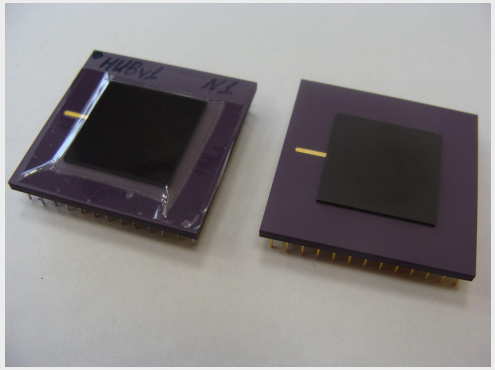
2) Prototype demonstrator for TPC

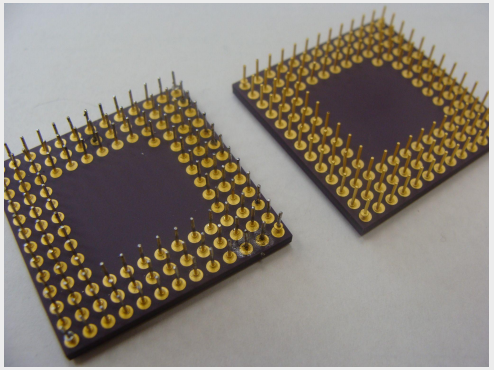
**Supporting components:**

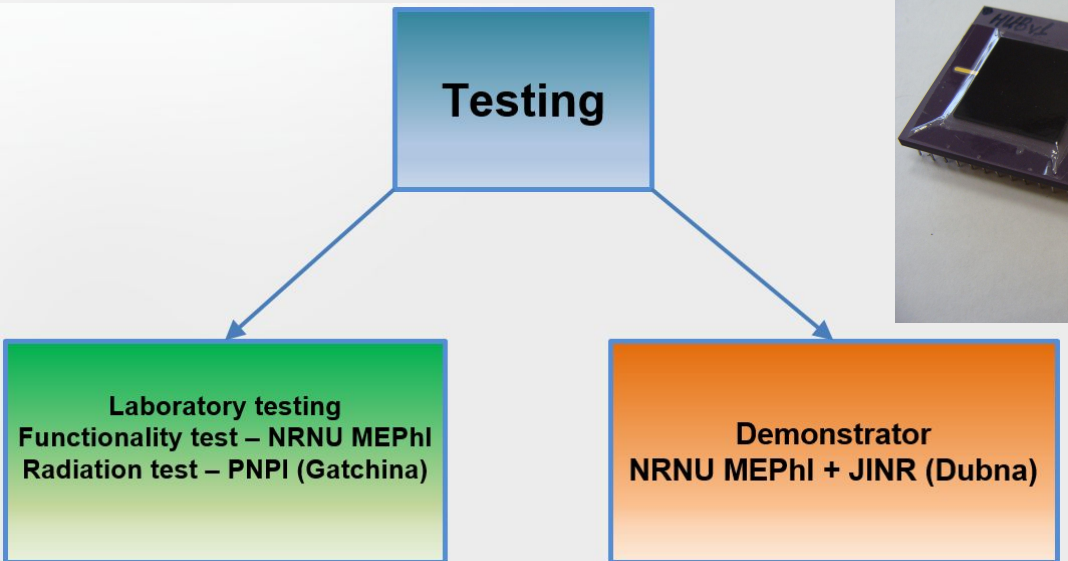
- SLVS – LVDS translators and passive components
- Comparators with adjustable hysteresis to evaluate CML eye-opening at different loads
- FMC HPC (on back side)

Hub v1 photos (chip & case)



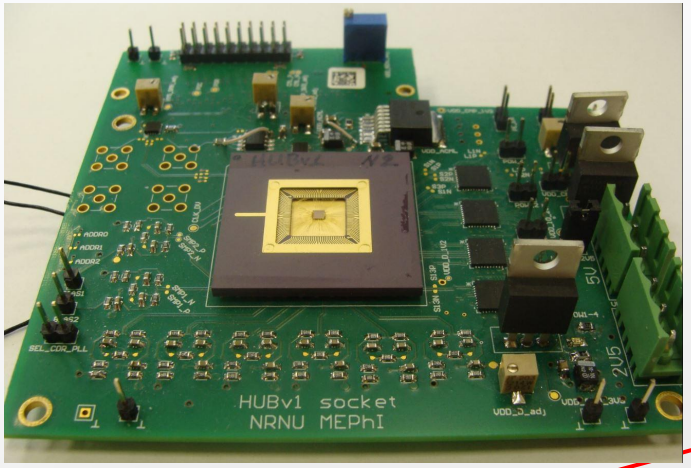





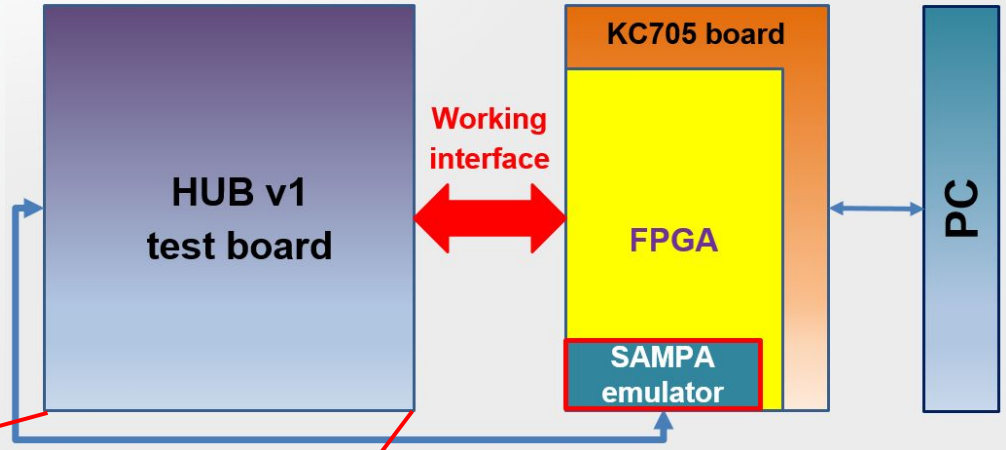


# Lab test bench

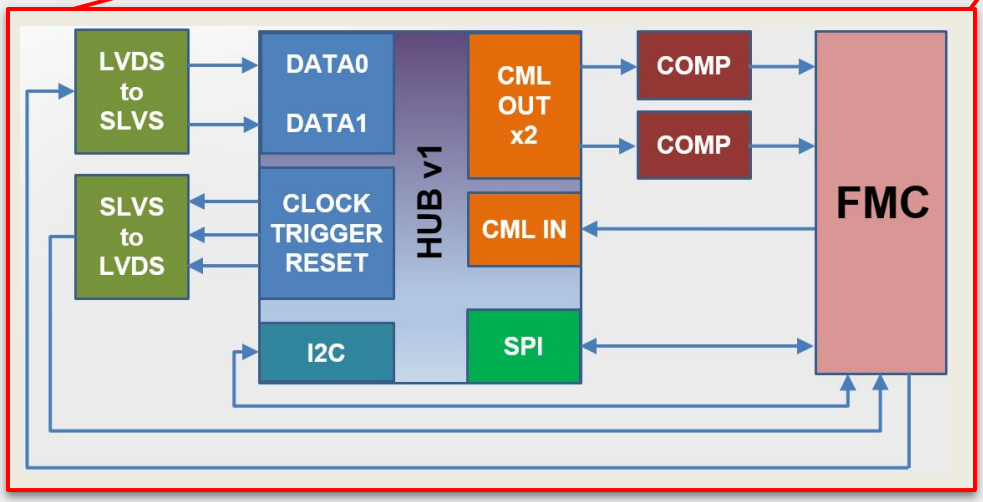
Hub v1 Test board




Hub v1 Test environment

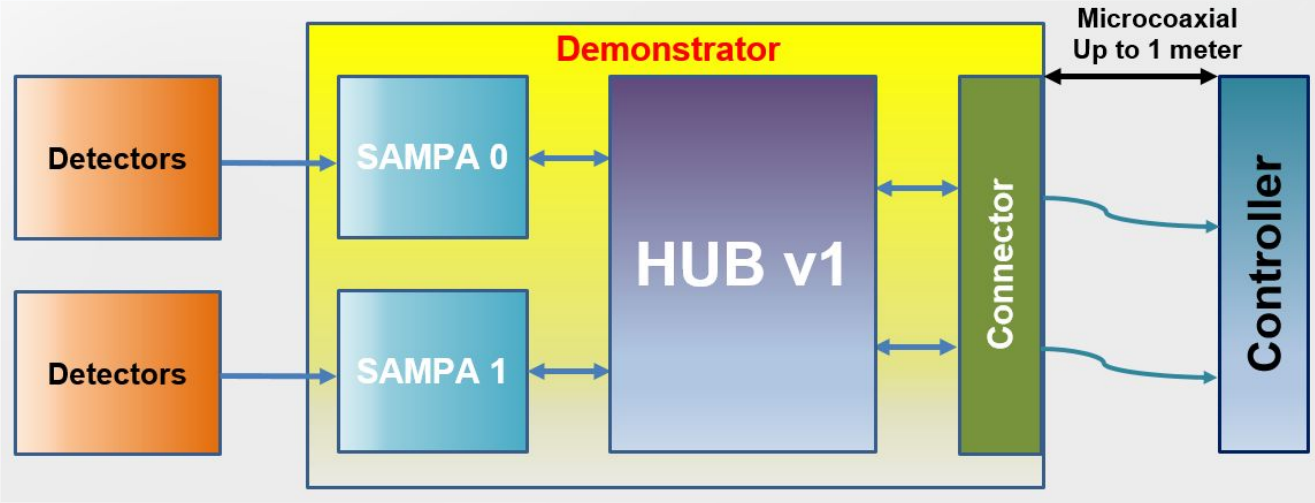



Test board block diagram

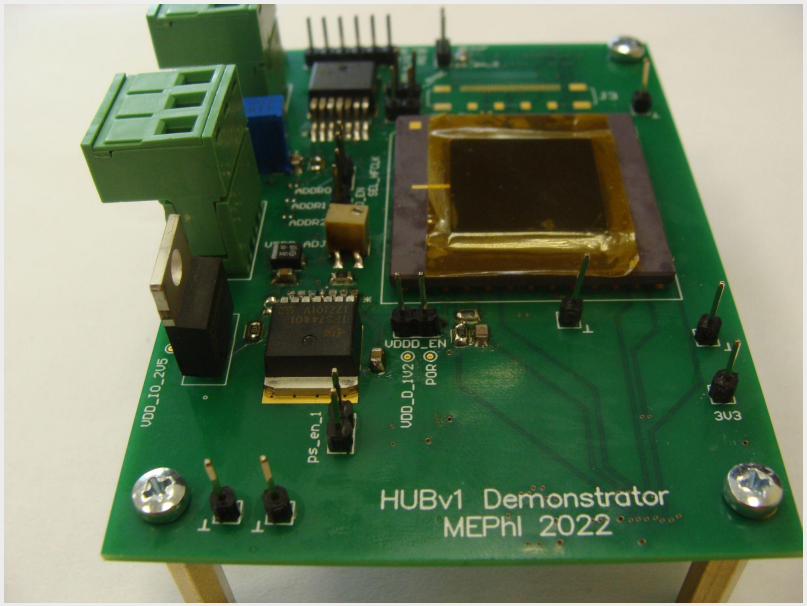



K705 board

# The demonstrator concept




Hub v1 Demonstrator environment

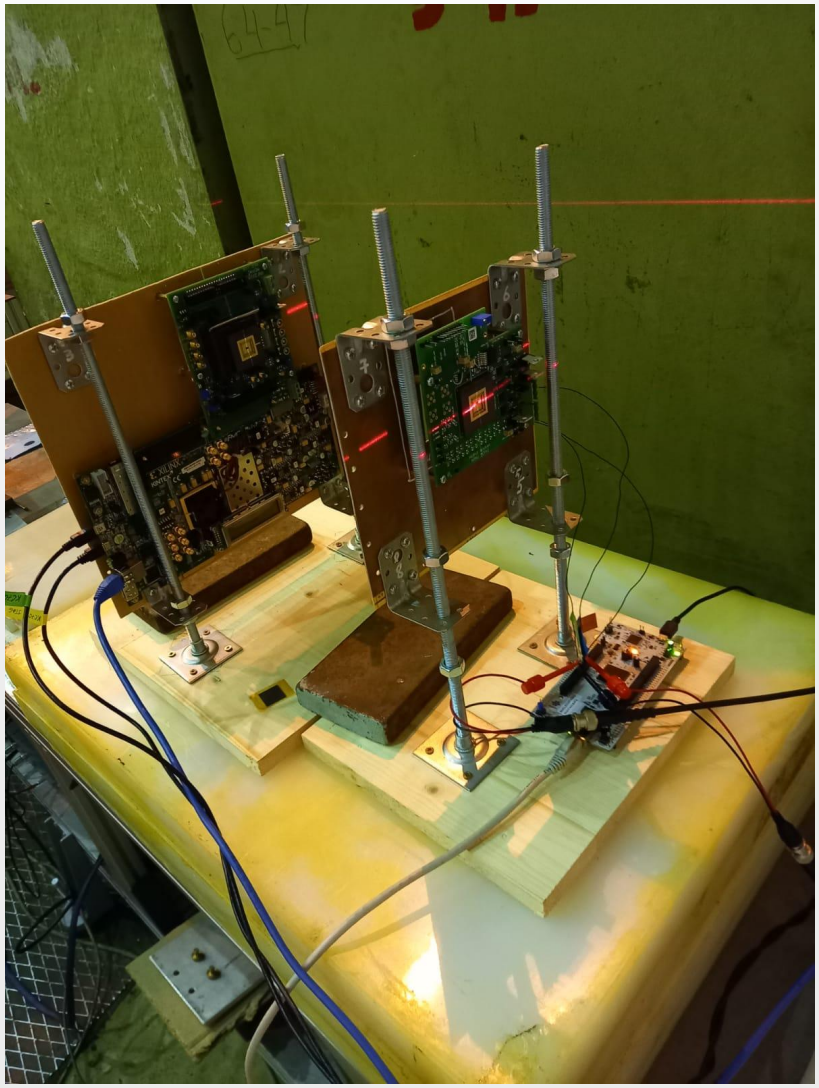


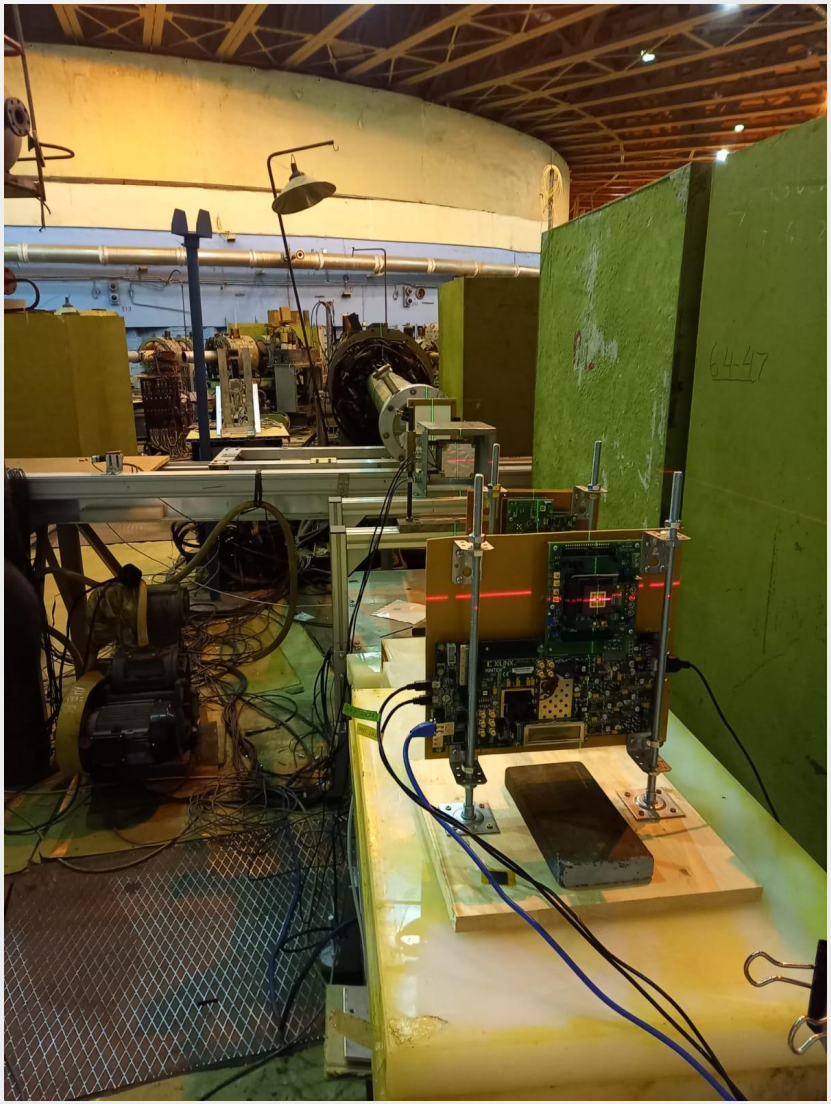

Hub v1 Demonstrator board

# The lab testbench in calibrated beam

Purpose - checking functionality of the chip blocks against heavy particles

Tests were done at PNPI, Gatchina in Feb. 2022



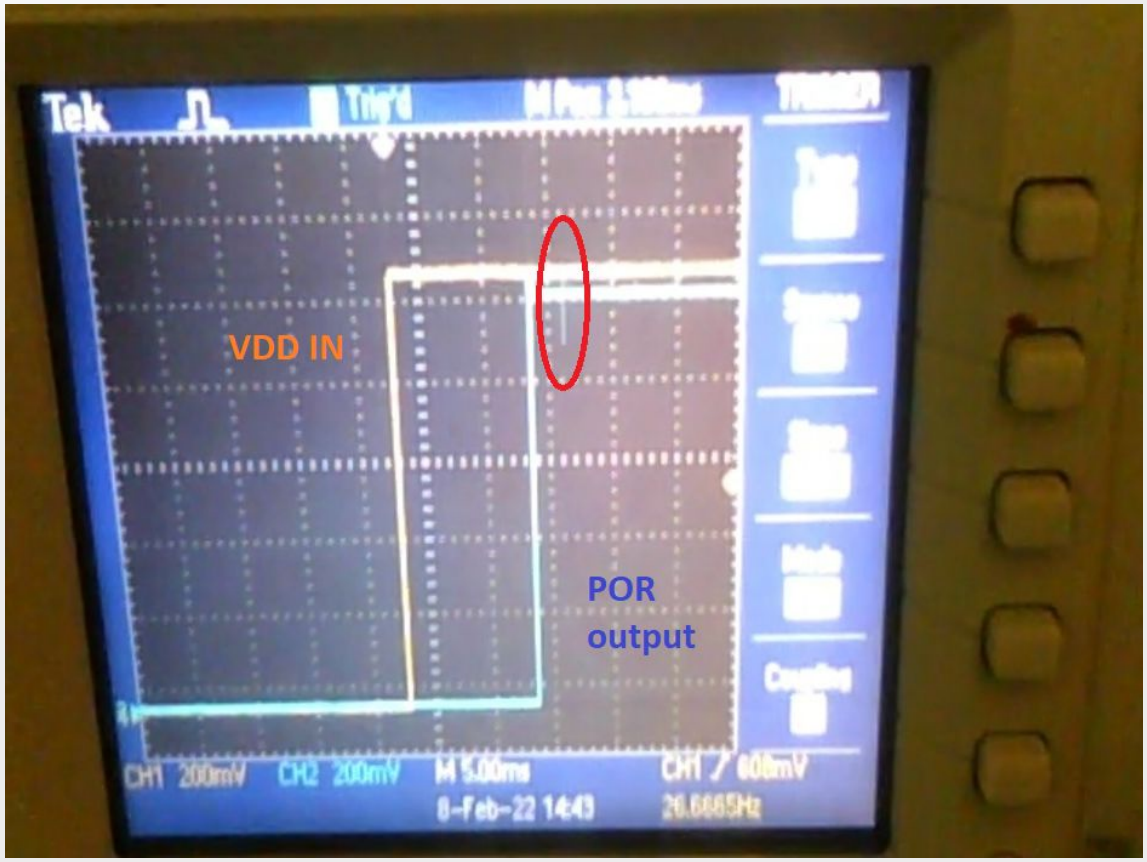


# First results

(interference records under irradiation)

2 types of test records:

- analog type (video record from scope to camera)
- digital one (signals, digitized by ADC) – now in data processing



# Test radiation environment

1) Radiation tests were performed in PNPI at Gatchina according to GOST 15.101-98
2) Bunch characteristics:
   a) particles, energy: protons, 1 GeV
   b) bunch diameter, uniformity: 19 mm, 5%
   c) fluence: $5 * 10^7$- $5 * 10^8$ particles / $cm^2$ / s
3) Experiment characteristics:
   a) Irradiation duration: 10 hours
   b) Average fluence: $2 * 10^8$ particles / $cm^2$ / s
   c) Total fluence: $2.54 * 10^{12}$

# Next steps on Hub chip

1) To remake the prototype chip in 90 nm CMOS process of Mikron fab at Zelenograd.
2) To design the second version of the chip in TSMC 65 nm PDK and submit it to the fab process via the integrator company (WaiFu IC, China).
3) Study chip caseless usage at board level. The flip-chip technique is not considered now
4) The chip should be a socket compatible with the manufactured Demonstrator board (one for Hub v1 chip) to be able to check functioning at MPD TPC

# Front-end project review

**Main goals:**

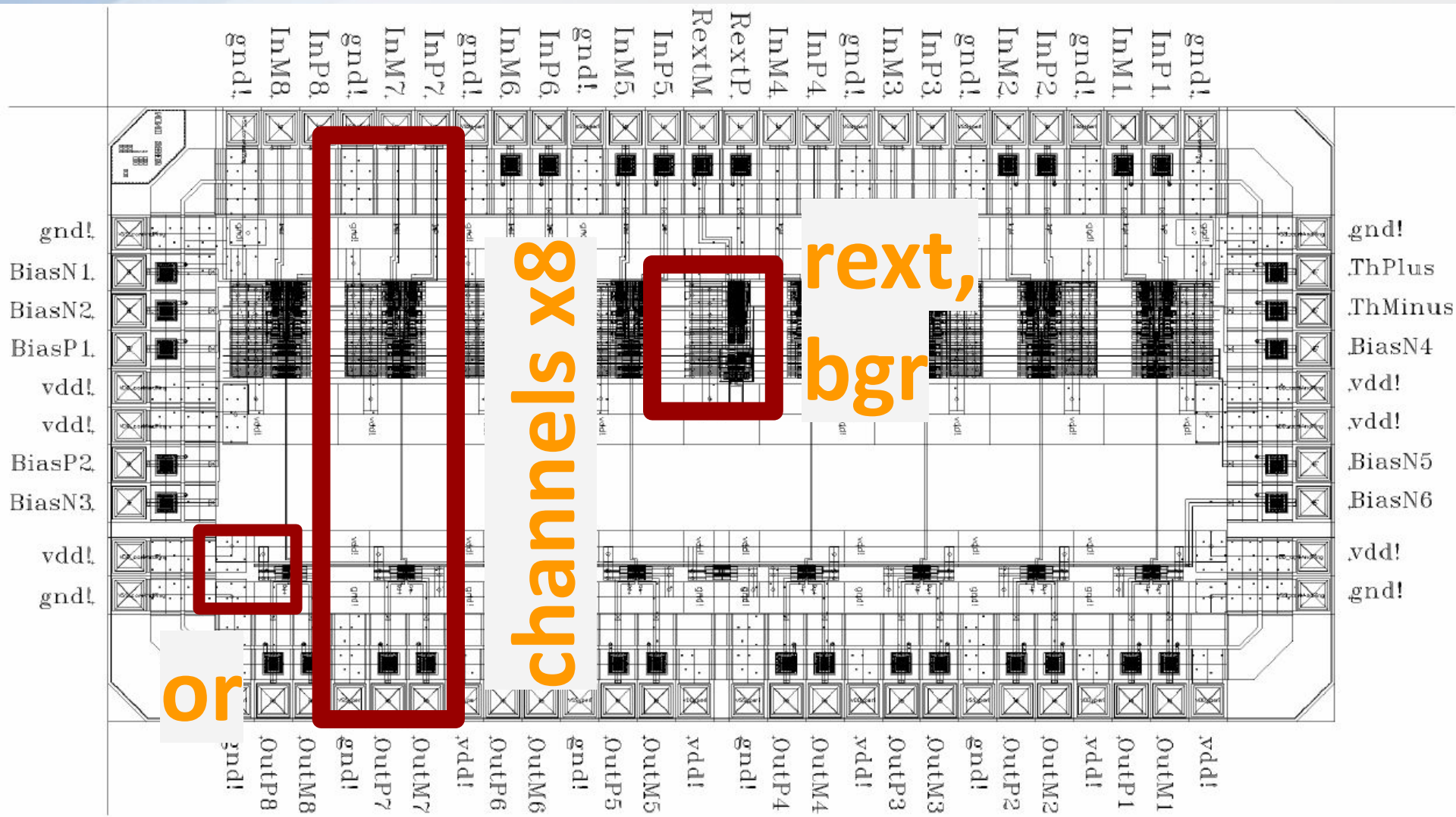
– Approbation of ASIC start-to-finish design route, relevant to 180 nm CMOS process HCMOS8D at Mikron fab in Zelengrad

– Design of building functional blocks for RPC front-end electronics

**ASIC design stages:**

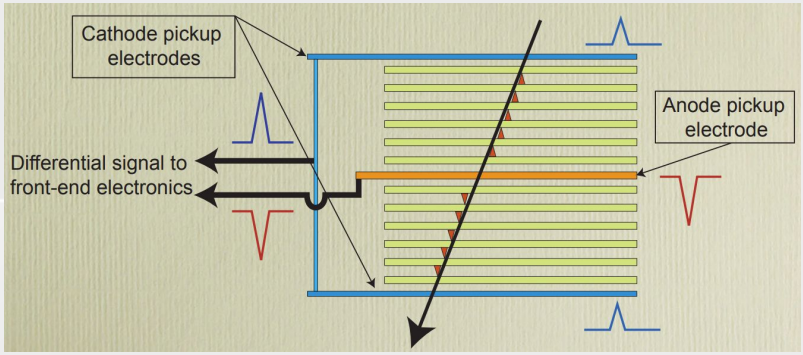
- Structural scheme and behavioral simulation
- Building blocks schematics design & integration
- Deadline for GDSII submission to the MPW run (25.08.2022)

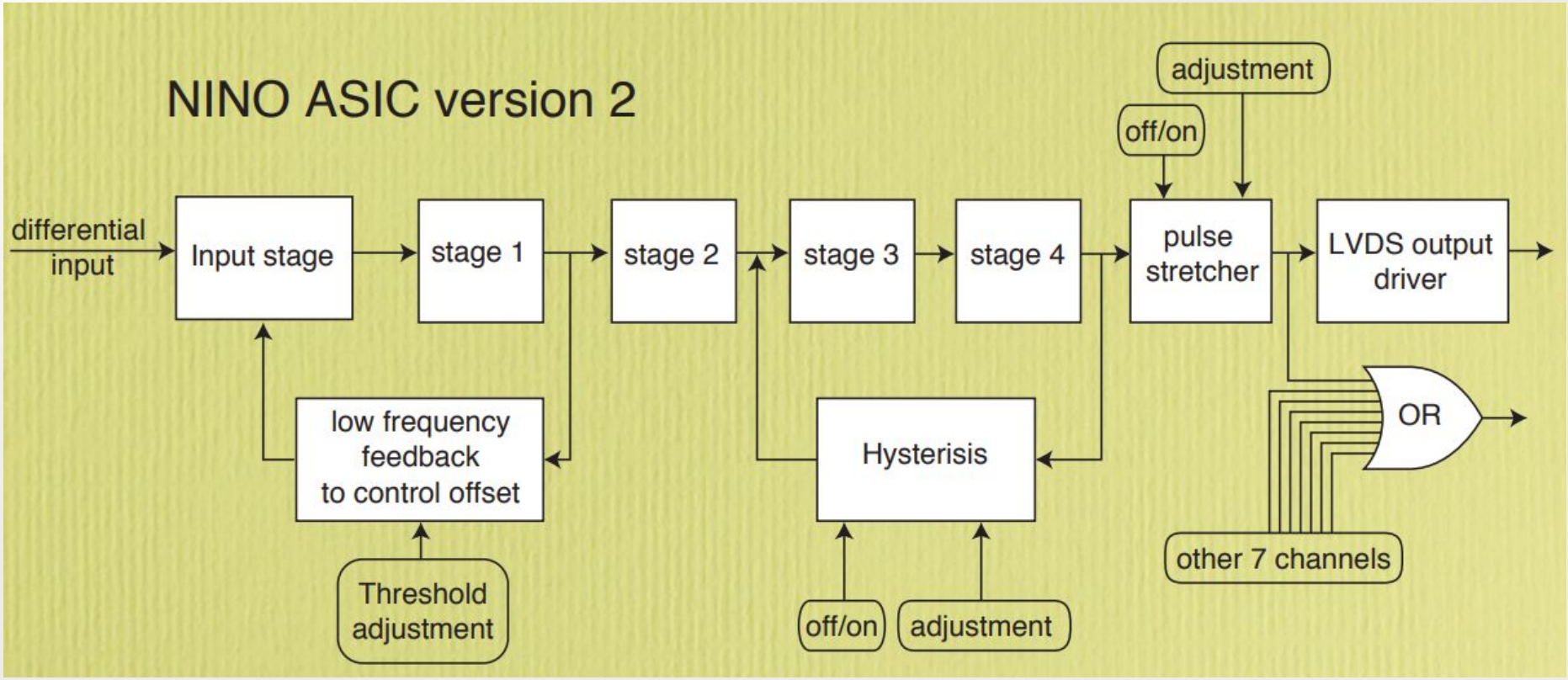
# ASIC layout




Functional analog and pin compatible with the design of NINO ASIC ( NIMA, Volume 533, Issues 1–2, 2004, pp. 183-187)

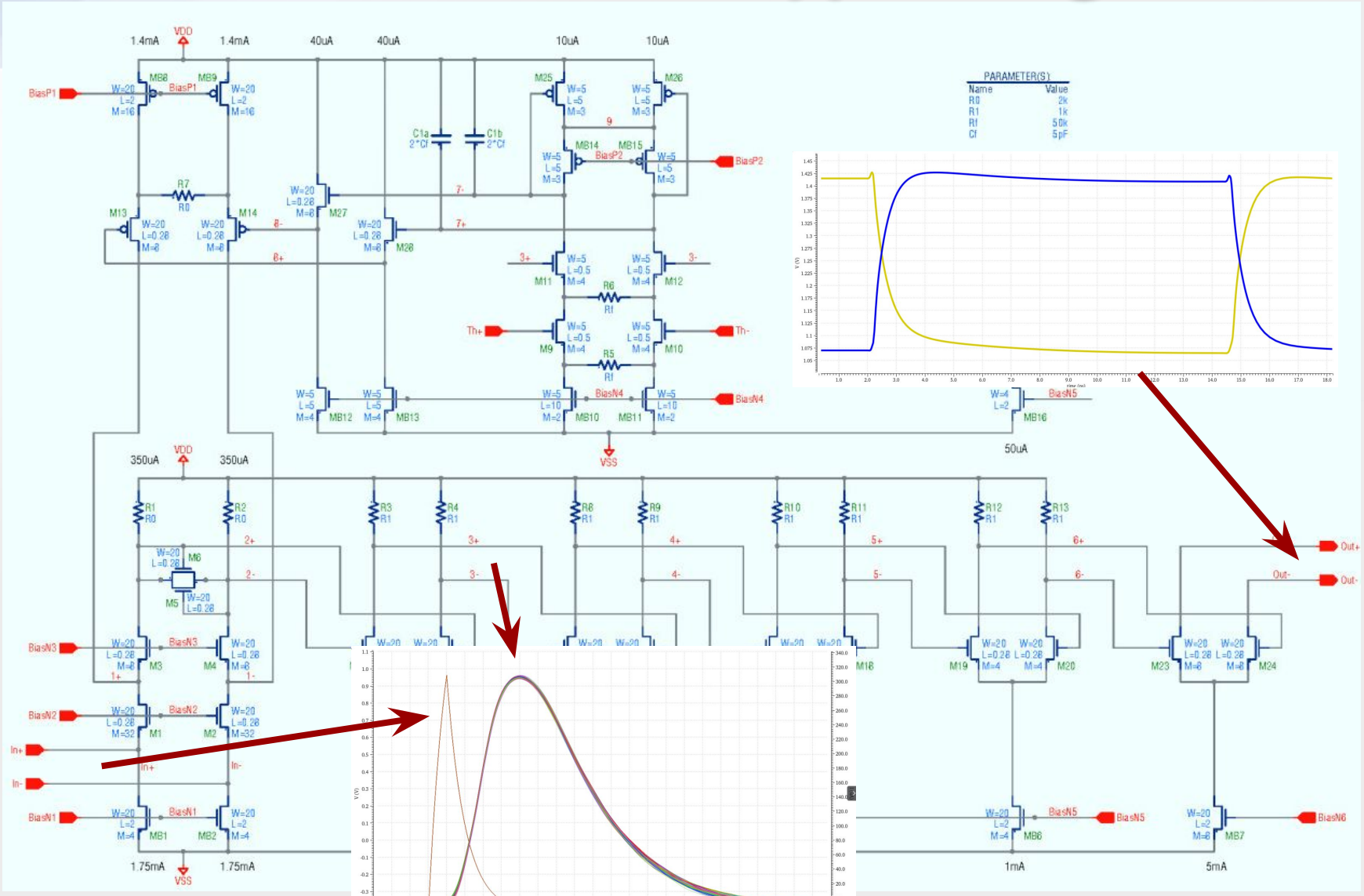
# Reference point




*F. Anghinolfi, P. Jarron, F. Krummenacher, E. Usenko, and M. C. S. Williams. NINO: An Ultrafast Low-Power Front-End Amplifier Discriminator for the Time-of-Flight Detector in the ALICE Experiment IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 51, NO. 5, OCTOBER 2004

# Channel structure & typical signals



# Main specifications

| Parameter | Value |
|---|---|
| Node | 180 nm CMOS of Mikron fab |
| VDD (IO, Core) | 1.8 V |
| Count of channels | 8 |
| Power consumption | 300 mW |
| Peaking time | 1 ns |
| Dynamic range | 30-2000 fC |
| Jitter | < 15 ps (rising), < 60 ps (falling) |
| Noise (Cdet=0) | < 2000 e |
| Rin adjustment | 35-60 Ohm |
| Threshold adjustment | 0 - 500 fC |

# Summary

- Presented is the current activity of MEPhI ASIC lab on chip design for experiments at NICA. Those are: 1) FEE chip for RPC and 2) data concentrator one

- FEE chip has been designed as functional analog of NINO ASIC (CERN, 2004-07). It is an 8-channel structure of fully differential amplifier-discriminator. The chip will be prototyped soon in 180 nm CMOS HCMOS8D process of Mikron fab, Zelenograd

- Data concentrator ASIC HUB has been developed according specifications of processing electronics for the MPD TPC. The main aim is uninterrupted processing and serialization of digital output data from two SAMPA FEE chips and their transmission via AWG-36 cables at the speed up to 2.56 Gbit/s