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Development of ASICs for experiments at NICA

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The results of development and laboratory testing of a prototype data concentrator integrated circuit (ASIC HUBv1) are presented. HUBv1 was developed for processing of signals from the detector chips of the time-projection chamber of the MPD experiment (NICA, Dubna). The main target of this ASIC is uninterrupted processing and serialization of digital output data from two SAMPA detector chips and their transmission via AWG-36 type cables up to 1 m long at the speed of 2.56 Gbit/s to the data acquisition controller board. Eight data and six SLVS clock ports are used to connect the SAMPA chips. The received data is error-checked using Hamming code and is available on the two high-speed CML output ports, each with bandwidth up to 2.56 Gbps. Both SAMPA and SIMC chips are controlled by issuing control commands via the high-speed CML or slow SPI interfaces. The HUBv1 prototype was manufactured using TSMC's 65 nm CMOS technology and packaged in CPGA120-type packages. The total power consumption of the ASIC does not exceed 500 mW. The results of laboratory testing of the chip and radiation resistance testing of the analog blocks are presented.

The development of key building blocks of a prototype application specific integrated circuit (ASIC) for the SPD experiment at NICA Nuclotron (Dubna) is presented. It was designed as an 8-channel fully differential amplifier-discriminator which could be used as a front-end electronics for resistive plate chambers as well as for time-of-flight measurements.

The ASIC has an architecture similar to the NINO chip developed at CERN. Each channel consists of the following functional blocks: a current preamplifier-shaper with the peaking time of 500 ps, low-frequency feedback with built-in threshold preset circuit, few additional amplification stages, pulse stretcher, LVDS output stage and some other supporting blocks. The chip is optimized for the input capacitance in range 1-10 pF, has adjustable threshold of 10-450 fC, and adjustable stretching time of 1-100 ns. The equivalent noise charge is not more than 2500 e at input capacitance up to 10 pF. The design was optimized for reducing front-edge jitter (less than 15 ps). Both schematic and layout of designed blocks are presented, simulation results are shown. PVT variation and Monte-Carlo mismatch plots are also given.

The development was conducted in the 180 nm CMOS process PDK of Mikron fab at Zelenograd. GDSII file was submitted to the factory at late August 2022.

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