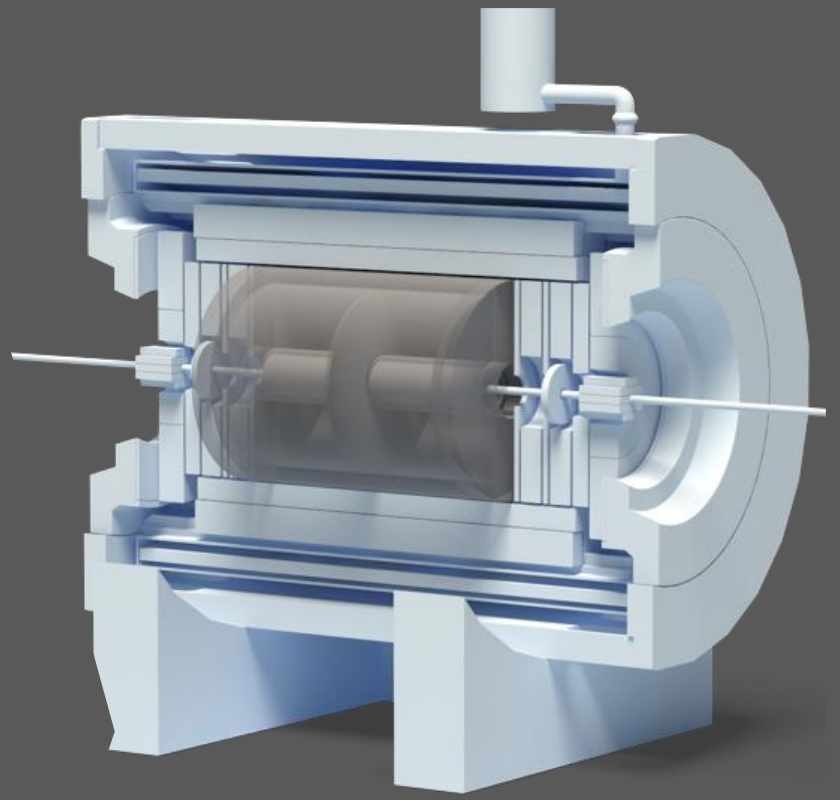
Data acquisition system of the TPC/MPD detector of the NICA project

Stepan Vereschagin, on behalf of the TPC/MPD group, VBLHEP, JINR



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NICA MPD

Outline

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- Data throughput estimates: slides 16-18
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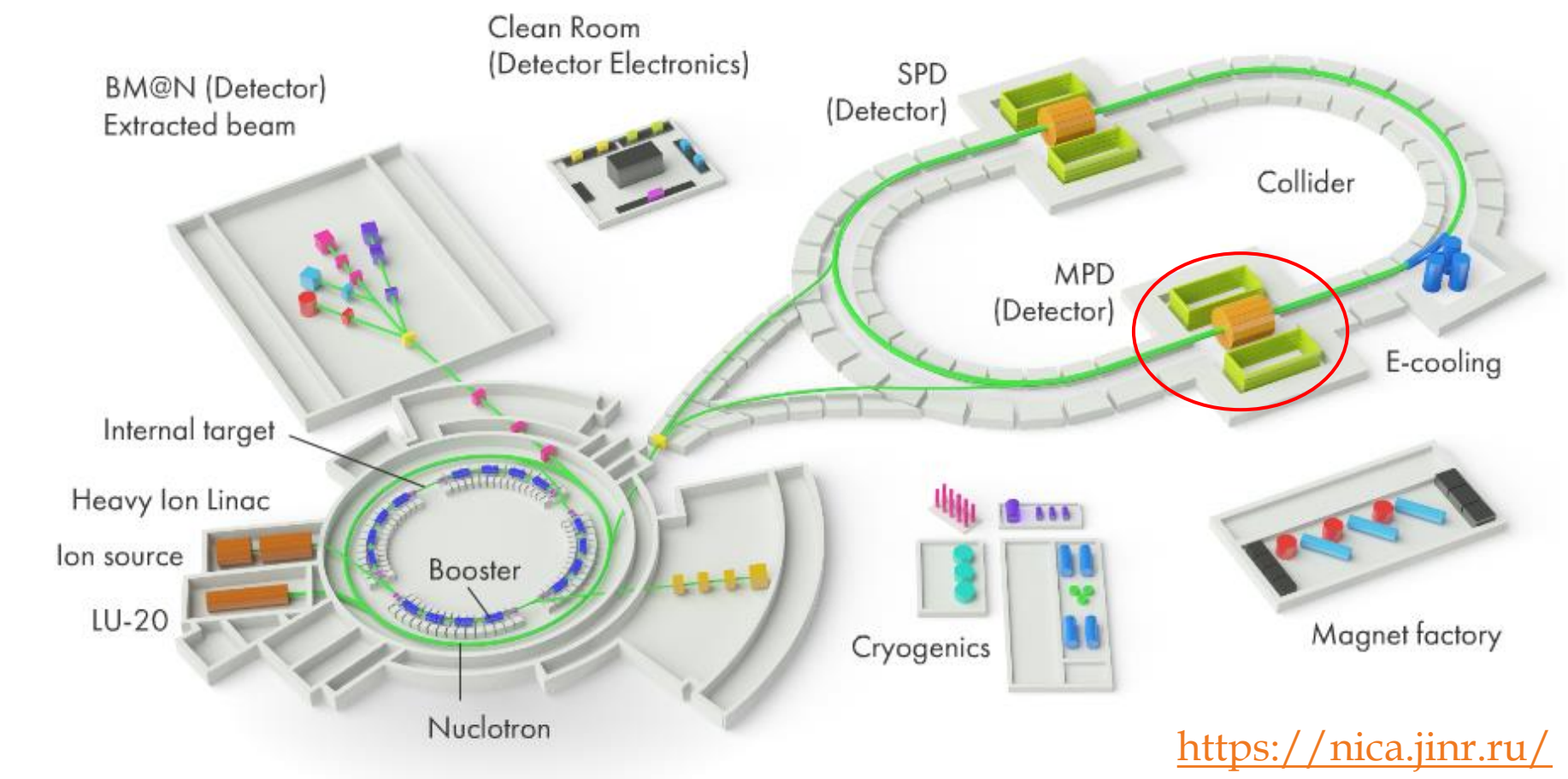
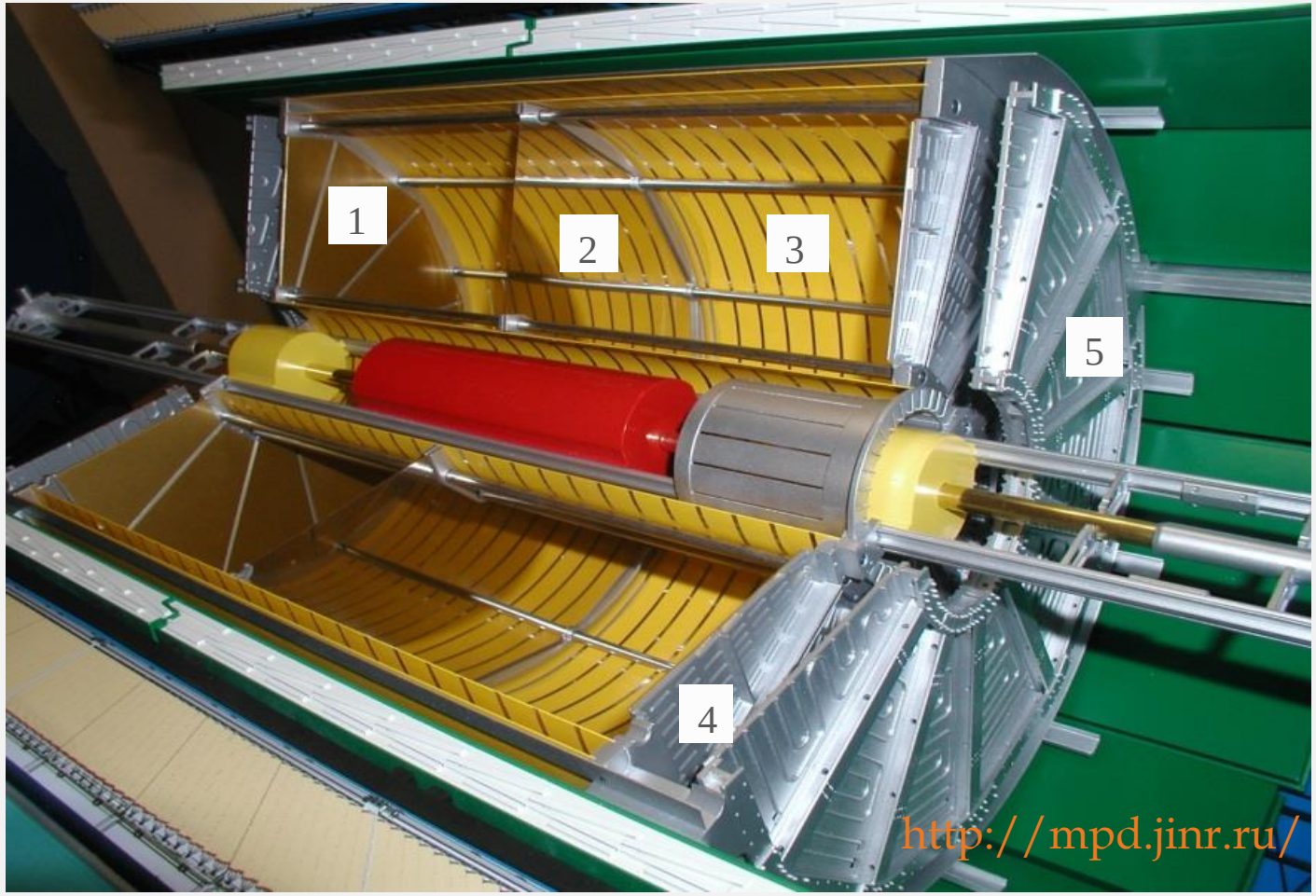
NICA Complex



https://nica.jinr.ru/

Central part of the MPD mock up with TPC cut



The TPC/MPD design requirements:

- The overall acceptance: $\eta < 1.2$
- The momentum resolution for charged particles is under 3% in the transverse momentum range $0.1 < pt < 1$ GeV/c
- Two-track resolution is of about 1 cm
- Hadron and lepton identification by dE/dx measurements: with a resolution better than 8%
- Operation trigger rate: 7 KHz

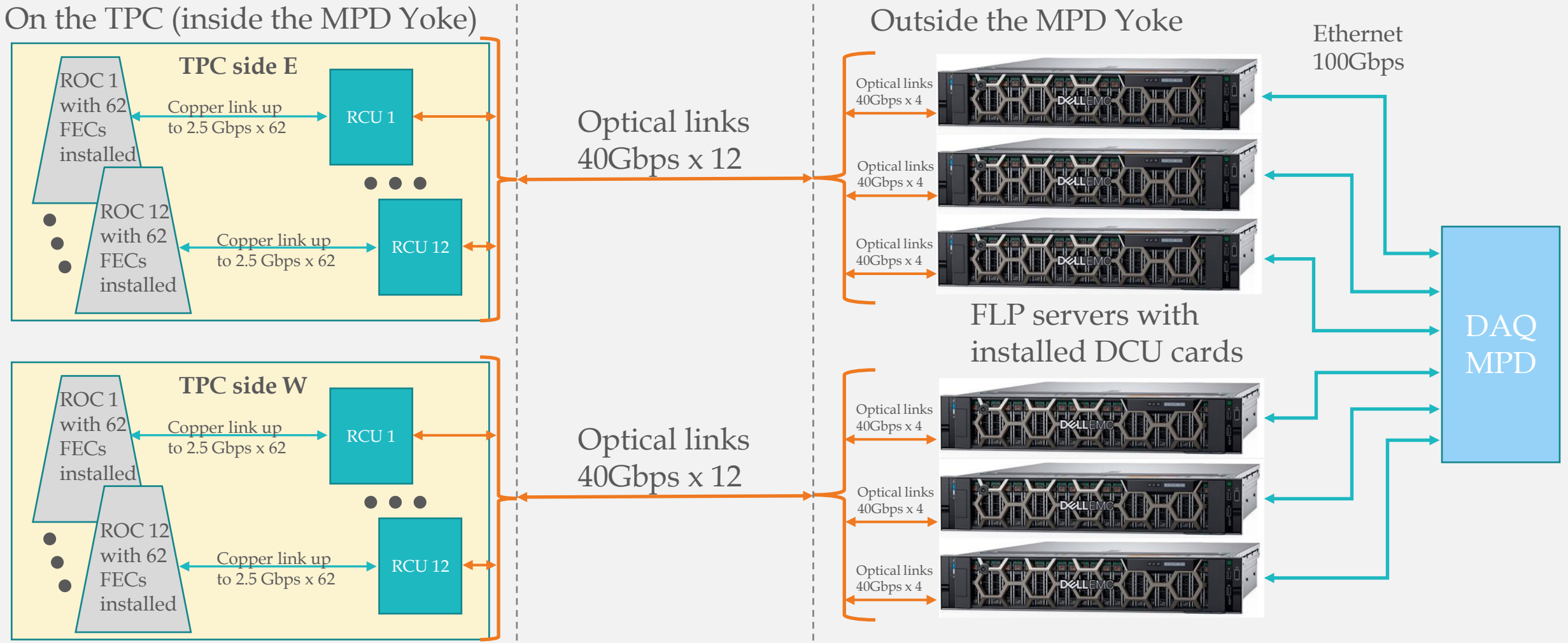
1 - MWPC;
2 - HV electrode;
3 - Field cage;
4 - FEE position;
5 - End cap thermal screen;

For details on the TPC look into the S.Movchan presentation: “MPD TPC status”

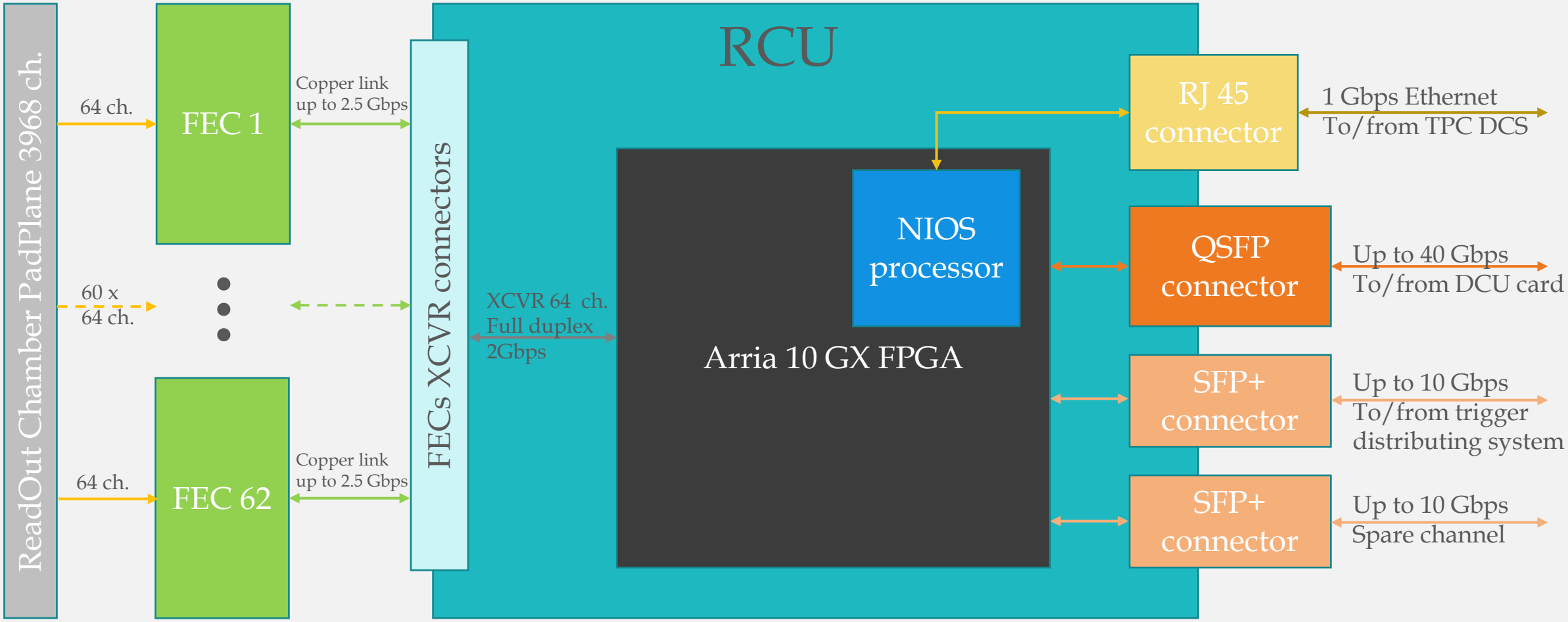
TPC/MPD data acquisition system main parts

- Front-End-Cards (FEC): 1488 pc., 95 232 10-bit ADCs in total
- Readout and Control Units (RCU): 24 pc. in total
- Data Concentrator Units (DCU): 6 pc. in total
- First Level Processor (FLP) servers: 6 pc. in total

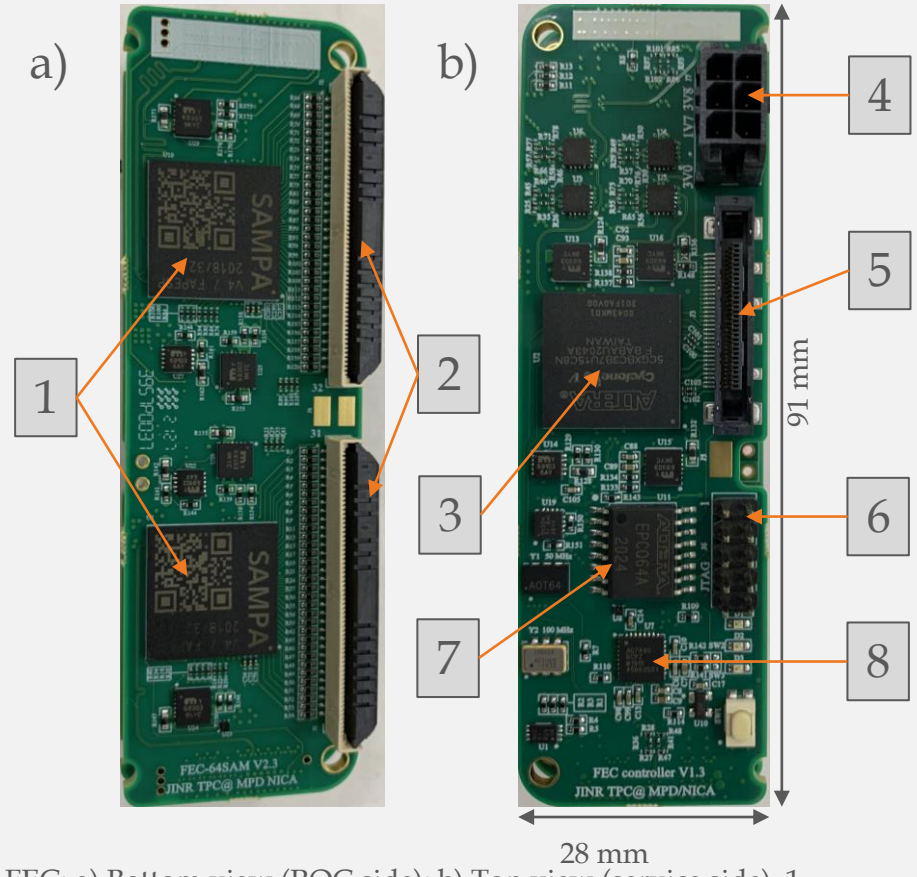
TPC/MPD DAQ conceptual scheme



One chamber readout scheme (1/24 of full TPC readout)



Front-End Card



FEC: a) Bottom view (ROC side); b) Top view (service side). 1 – SAMPA ASICs; 2 – input connectors; 3 – FPGA; 4 – PS connector; 5 – HSSI connector; 6 – JTAG connector; 7 – EPCQ64 flash memory; 8 – control 16 ch. ADC.

- The total number of registration channels: 64
- Maximum input charge in a linear range: 100 fC
- ADC resolution: 10 bit
- ENC: les than 1000 e^-
- Readout serial interface: up to 2.5 Gbps
- The total number of monitored values of current, voltage, and temperature: 16

➢SAMPA chips management via FPGA high speed interface

➢*Double-PCB FEC provides opportunities for possible upgrade of the card readout.*

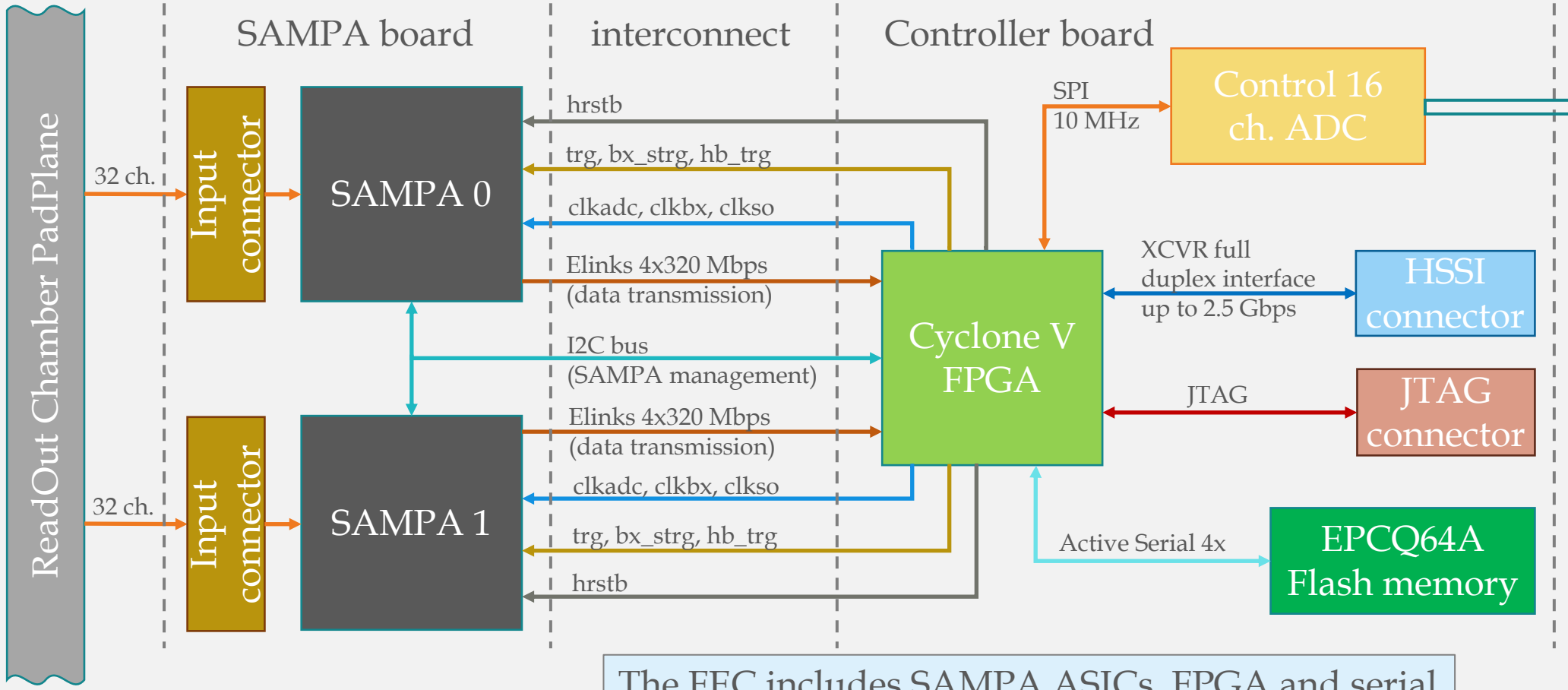
➢*Transfer of data and trigger signals was realized with the same high-speed serial interface.*

➢*Onboard circuit and embedded protection functionality against SEU are provided.*

➢*Remote system update for FEC firmware was provided.*

Double-desk FEC formfactor:
a) SAMPA board;
b) Controller board;

FEC structural scheme

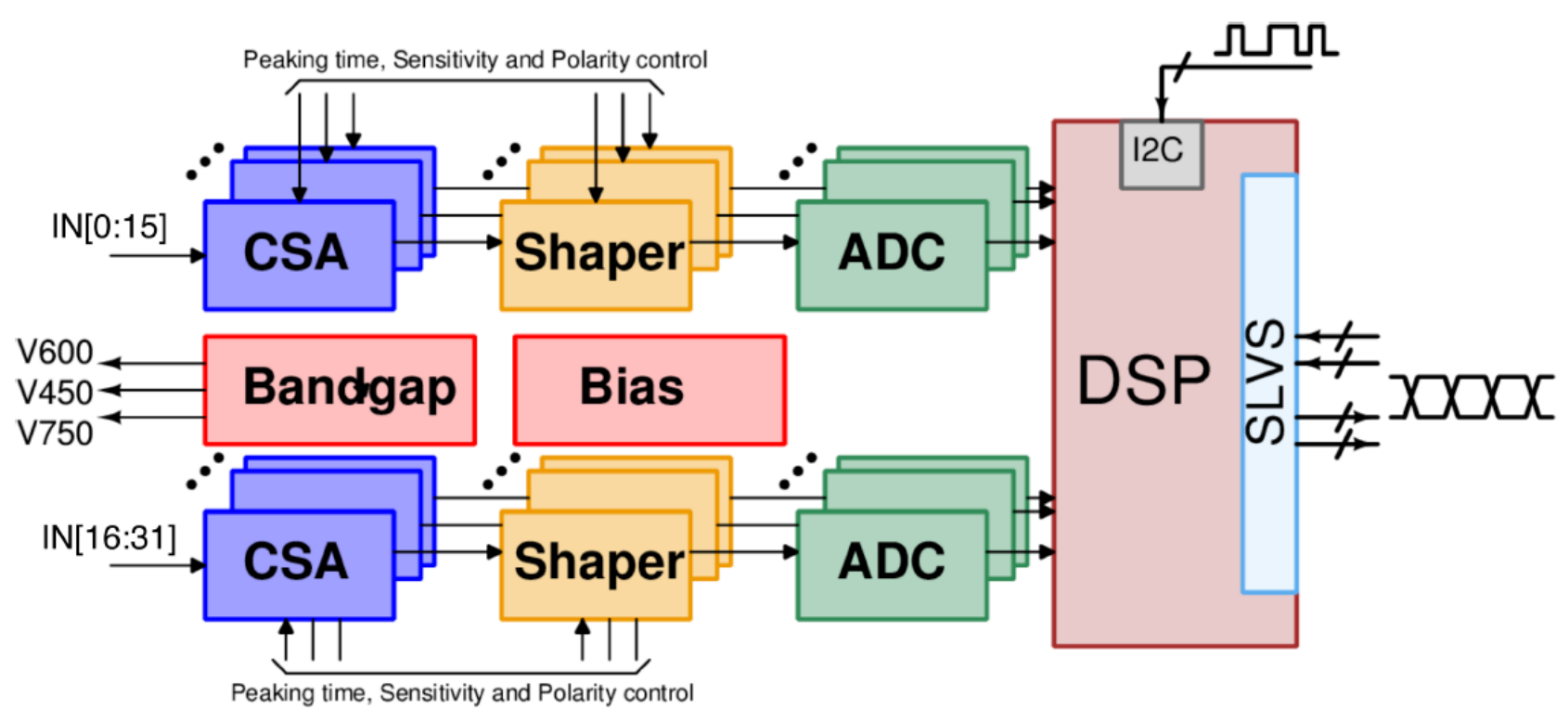


Control ADC data

```
{Temp     C5} 57.4
{1.7  V   in} 1721
{1.1  V   C5} 1102
{1.25 Vd  S0} 1249
{Curr2    S0} 299
{Curr1    S0} 8
{1.1  Vr  S0} 1101
{1.25 Va  S0} 1250
{Curr0    S0} 208
{Temp    Sam} 59.5
{1.25 Va  S1} 1248
{Curr3    S1} 200
{1.1  Vr  S1} 1102
{Curr4    S1} 8
{Curr5    S1} 292
{1.25 Va  S1} 1249
```

The FEC includes SAMPA ASICs, FPGA and serial interfaces.

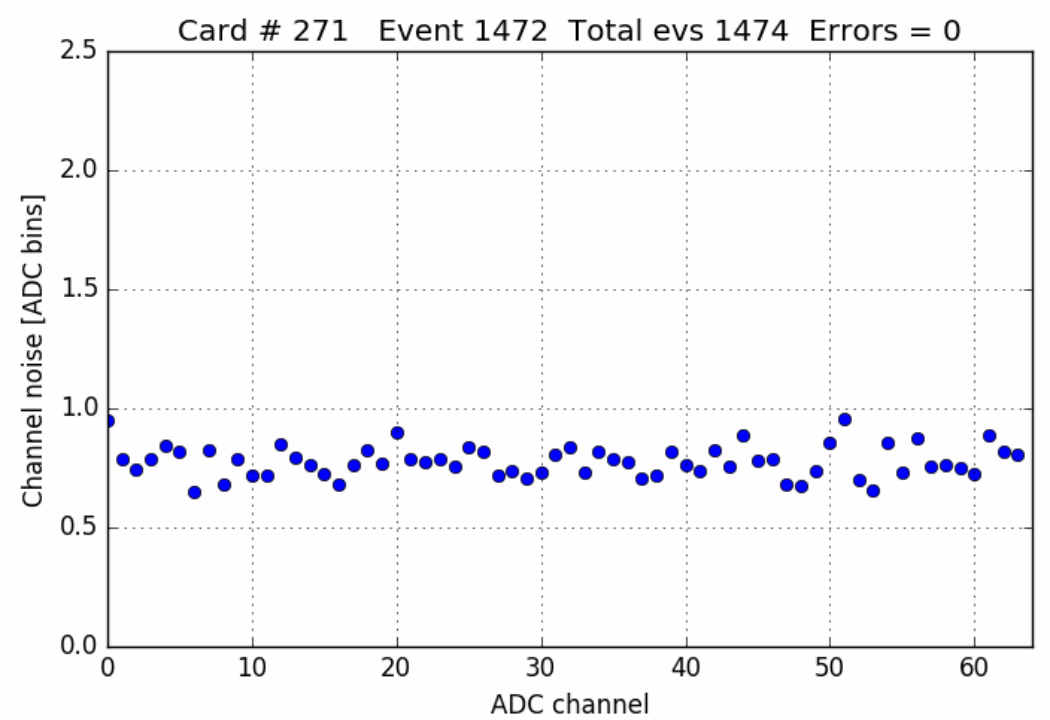
SAMPA ASIC: the core of FEE



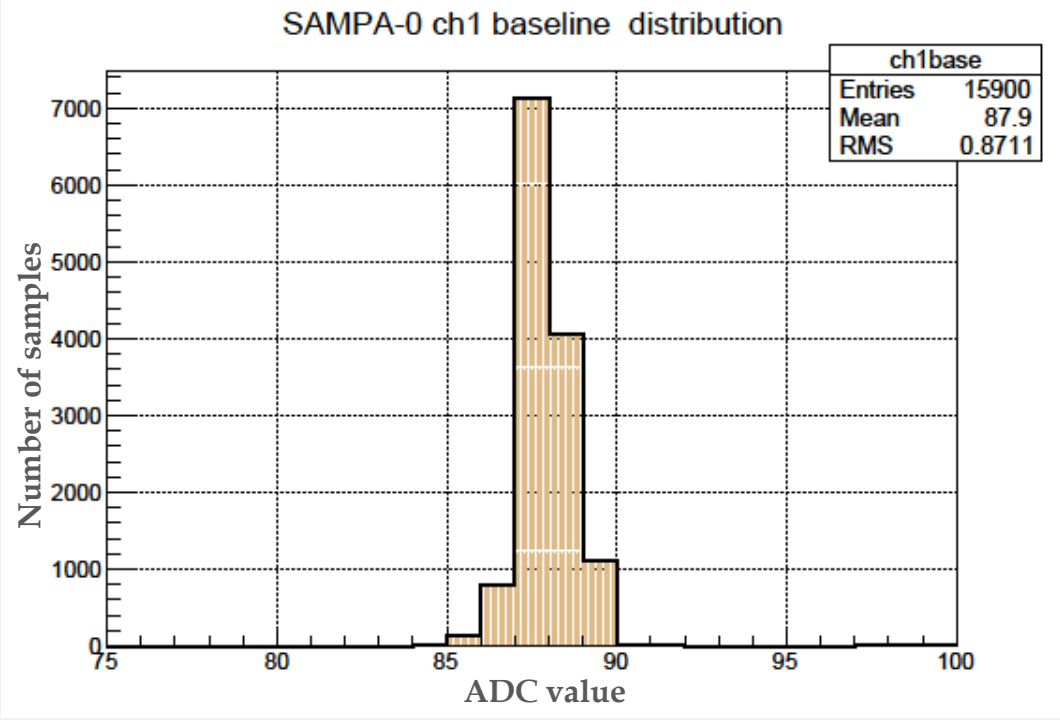
SAMPA ASIC includes 32 blocks of: charge-sensitive amplification, signal shaping, digitization, digital signal processing, data memory and serial data interface.

[1] J. Adolfsson, et al., SAMPA chip: the new 32 channels ASIC for the ALICE TPC and MCH upgrades, JINST 12 (04) (2017) C04008.

FEC noise measurement



Noise distribution over FEC channels

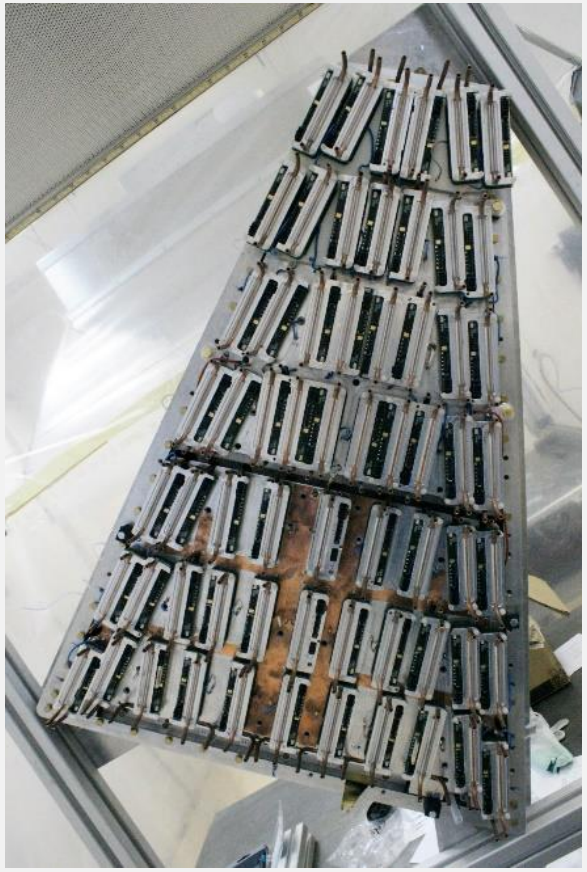


Typical noise distribution of a SAMPA channel

Measurement was done without FEC connection with ROC.
The measurements corresponds to SAMPA ASIC specification

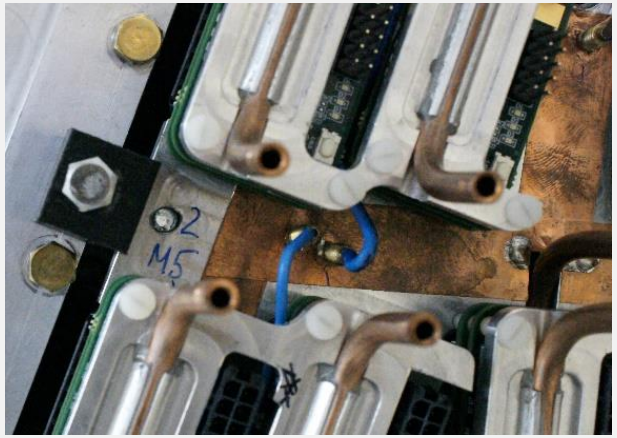
1 ADC LSB = 670 e^-

FECs integration on the ROC

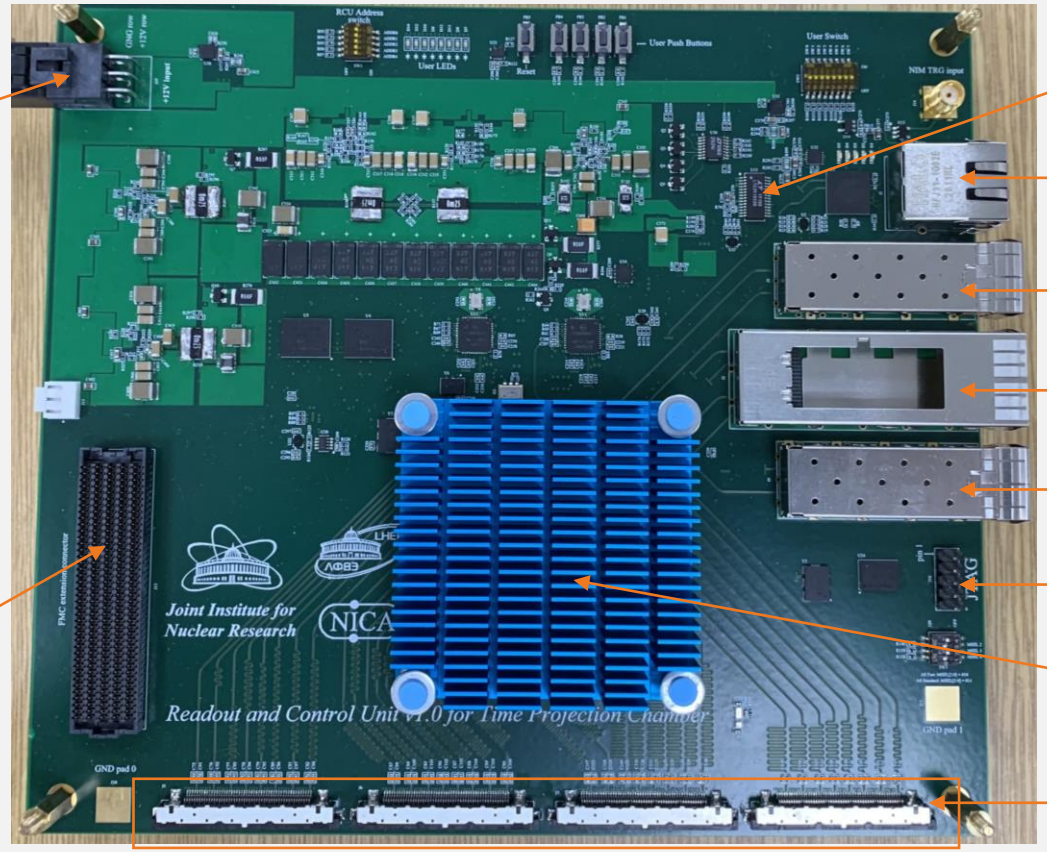


Double-desk FEC formfactor allows us to reduce amount of material at the TPC endcaps and to distribute it evenly.
All FECs where placed in one level covered from both sides by cooling plates.

Possibility for FECs additional grounding was provided.



Readout and Control Unit



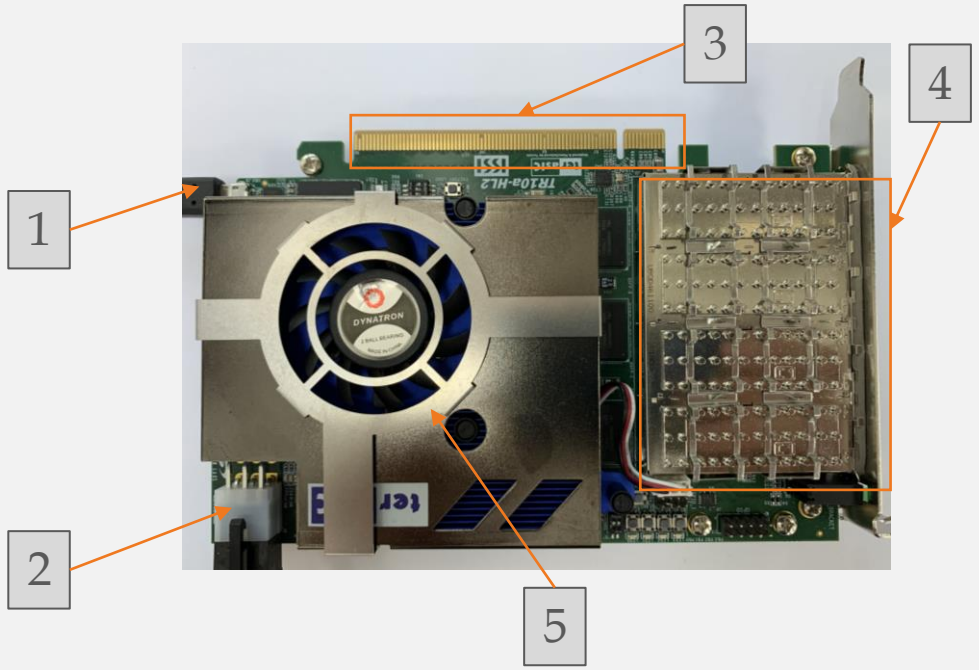
1. PS connector (+12 V)
2. 16-ch. ADC (health monitoring)
3. RJ45 connector (NIOS Ethernet 1Gbps)
4. SFP+ connector (optical trigger up to 10 Gbps)
5. QSFP connector (data transfer interface up to 40 Gbps)
6. SFP+ connector (spare optical channel up to 10 Gbps)
7. JTAG connector (FPGA programming end debugging + spare management channel)
8. Arria 10 GX FPGA
9. FECs XCVR connectors 64 full duplex channels
10. Multifunctional connector with GPIO pins and 2 spare XCVR

Main **RCU** functionality:

- Receiving data packets from 62 FECs;
- Buffering data with subsequent transmission to the DCU via optical channel;
- Organizing high-speed management channel to the FECs;
- Organizing FECs synchronization;

Data Concentrator Unit and First Level Processor server

+



DELL R740XD server

Receiving data via PCIe of the DCU card and after transmitting it to the MPD DAQ via 100G Ethernet

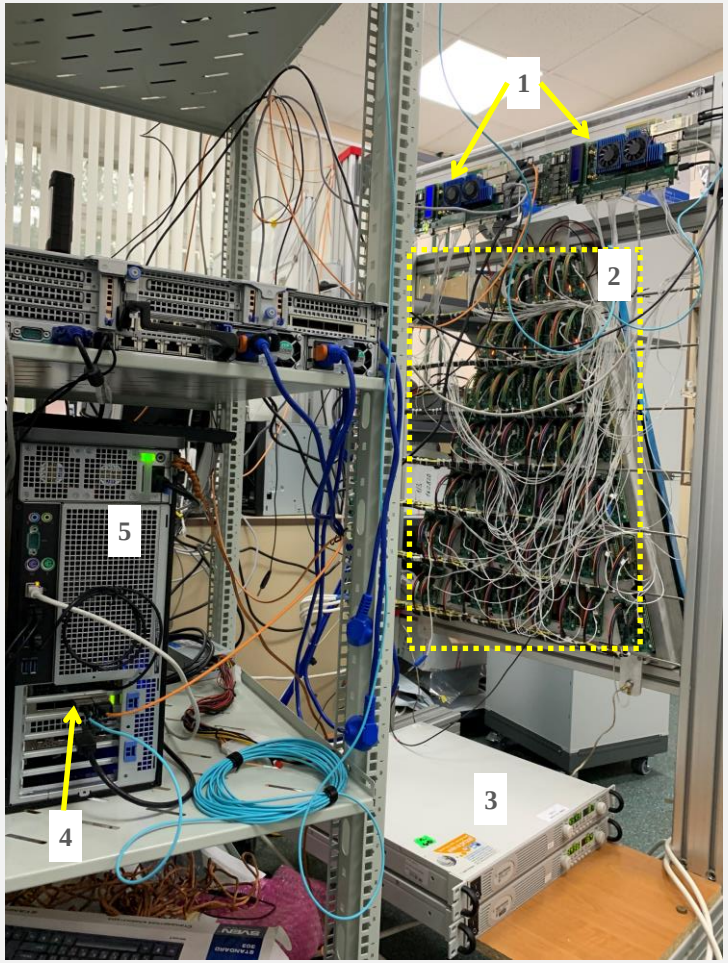
DCU card based on **Terasic TRHL2** development board

1) USB connector for onboard usb-blaster;
2) PS connector +12 V;
3) PCIe gen 3 x16 connector (double x8);
4) 4 QSFP connectors for data taking and management;
5) Arria 10 GX FPGA;

Main **DCU functionality**:

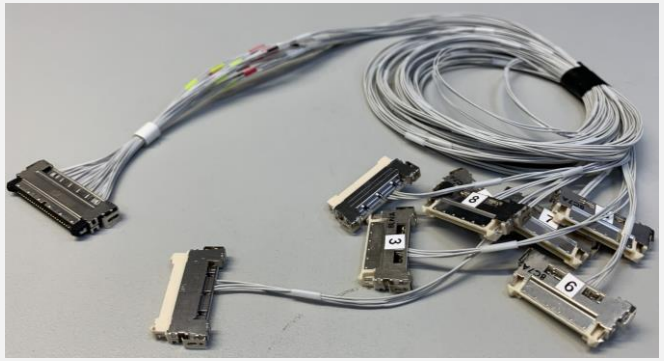
- Receiving data packets from four RCUs;
- Organizing high-speed management channel via PCIe;
- Managing of all downstream devices (RCUs, FECs);
- Buffering data with subsequent transmission to the server memory via PCIe ;

ReadOut Chamber DAQ test setup

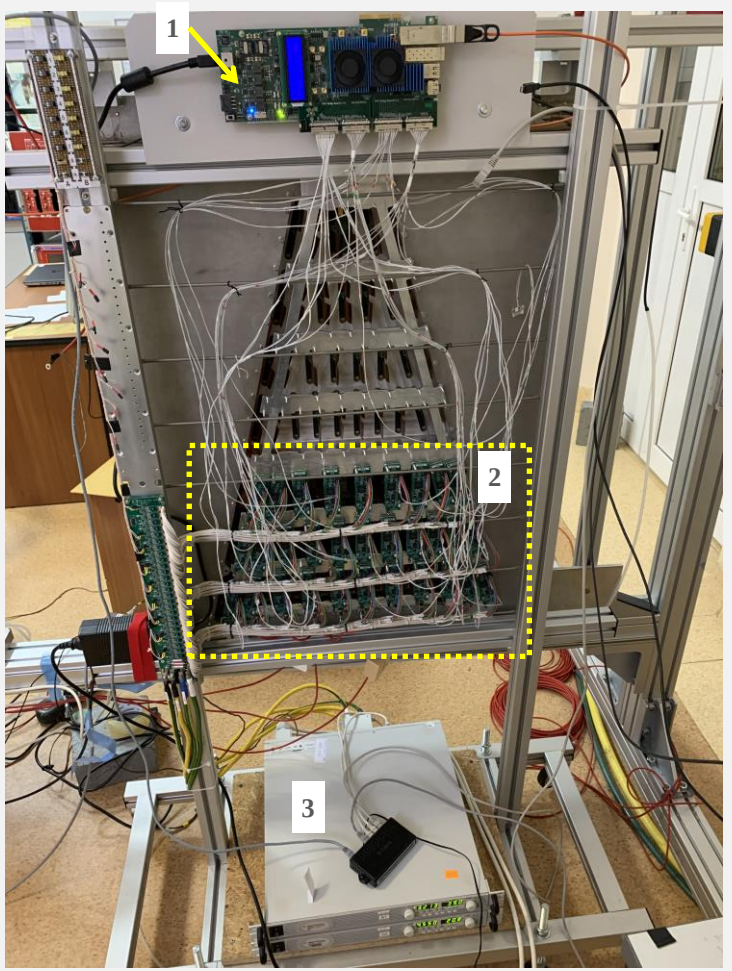


Test setup at building 201, VBLHEP

1. RCU prototypes
2. FECs on the ROC (62 pc. left and 31 pc. right)
3. LV power supply
4. DCU card connected with RCUs via fibers
5. Readout server



Vital element of the ROC data acquisition system is microcoaxial cable assembly based on μcoax 36 AWG cables and Hirose FX15, FX16 series connectors.



Test setup at building 40, VBLHEP

Data throughput estimate: FEC to RCU

- For 1 ch. raw event size is 301 10-bits samples + 50 bits header = 3050 bits;
- In FEC (64 ch.) data is packaged into 32-bits packets with small redundancy. Size of outgoing one event packet from FEC is: 6528 of 32-bit words = 208896 bits;
- Working with trigger rate 7 kHz data stream of one FEC is about 1.5 Gbps
- FEC provides 2 Gbps nominal data throughput, and taking into account 8/10 bit coding redundancy of 20% effective data throughput is 1.6 Gbps which is enough for data transmission at trigger rate 7 kHz.
- Used Cyclone V XCVRs upper data throughput limit is 2.5 Gbps. There is a possibility to increase effective data throughput from 1.6 Gbps to 2 Gbps by tuning FPGA's firmware;

Data throughput estimate : RCU to DCU

- For data transmission from each group of 16 FECs we use 1 optical channel of 10 Gbps (QSFP 40 Gbps = 4 x 10 Gbps) with effective data throughput of 8 Gbps (without 20% redundancy of 8/10 bit coding);
- For 16 FECs raw event size is 6528 of 32-bit words x 16 FECs = 104 448 of 32-bit words or 3 342 336 bits;
- 8 Gbps / 3342336 bits = 2.39 kHz – max trigger rate for raw events;
- The RCU will transmit data at trigger rate 7 kHz in a zero suppression mode;

Data throughput estimate : DCU to FLP

- For data transmission from two groups of QSFP optics (data from 2 RCUs) we use 1 PCIe 3.0 x8 with effective data throughput of 63 Gbps (without 1,5% redundancy of 128/130 bit coding);
- For two RCUs raw event size is 6528 of 32-bit words x 62 FECs x 2 RCUs = 809472 of 32-bit words or 25903104 bits;
- 63 Gbps / 25903104 bits = 2.43 kHz – max trigger rate for raw events;
- The DCU will transmit data at trigger rate 7 kHz in a zero suppression mode;

Summary

- Data acquisition system of the TPC based on ASICs, FPGAs, high-speed serial copper and fiber serial transmission lines.
- Usage of FPGAs gives an opportunities for tuning and upgrade of the system.
- Two DAQ equipped ROCs is now under testing at VBLHEP JINR.
- The DAQ system can operate at trigger rate 2.39 kHz in raw event mode and 7 kHz in a zero suppression mode.

Thank you for your attention!