The time synchronization of the ALICE Fast Interaction Trigger detector

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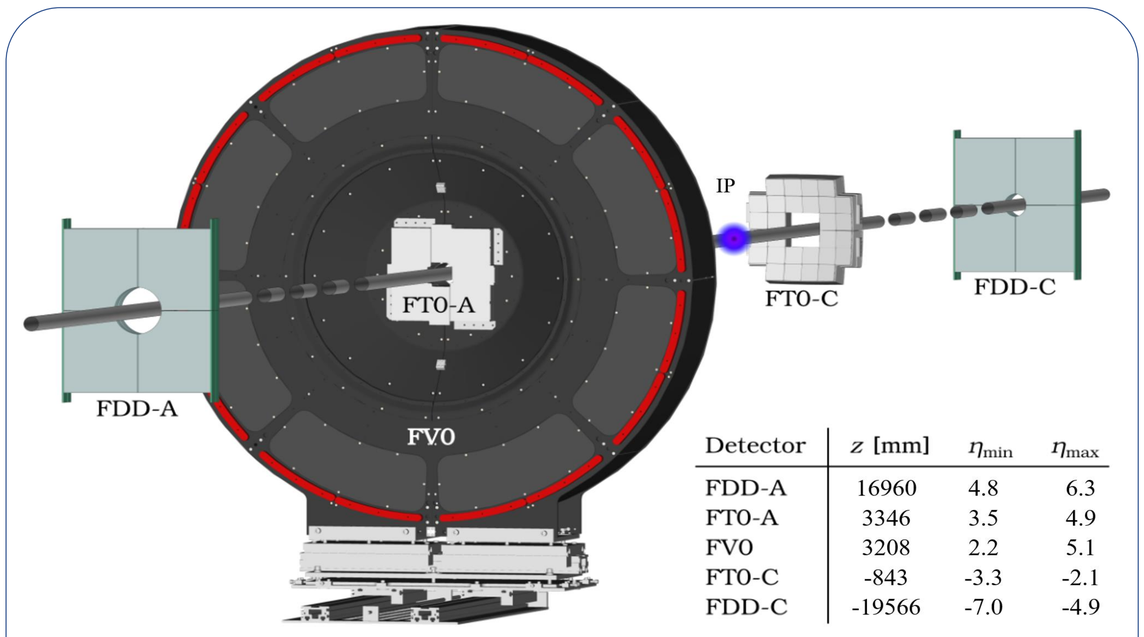
The Fast Interaction Trigger (FIT) detector produces online trigger signals, monitors luminosity and background, and is used in offline for calculation of the collision time, the event plane and the first indicator of the vertex position of the ALICE experiment at CERN during Run 3 of the LHC. The FIT consists of three subsystems: FT0 – a set of two fast Cherenkov arrays, FV0 – a large segmented scintillator disk and FDD (Forward Diffractive Detector) – also a scintillator located at very high pseudorapidity. All three subsystems (FT0, FV0 and FDD) use a single design of the front-end electronics consisting of "Trigger and Control Module" (TCM) and "Processing Module" (PM) with CFD, TDC and ADC parts. The collected data is processed in FPGA. Hit time measurements are done relative to the LHC high-quality clock with a time resolution of 25 ps for single MIP (Minimum Ionization Particle) and 8 ps for high multiplicity events. FIT FEE is connected to ALICE DAQ with GBT links for timestamps distribution and measured data sending.



Detector	z [mm]	η_{min}	η_{max}
FDD-A	16960	4.8	6.3
FT0-A	3346	3.5	4.9
FV0	3208	2.2	5.1
FT0-C	-843	-3.3	-2.1
FDD-C	-19566	-7.0	-4.9

Figure 1. Layout of the FIT detector: FT0, FV0, FDD subsystem. FT0-A, FV0, FDD-A and FT0-C, FDD-C are placed at opposite sides (A-side, C-side) of the interaction point (IP). Distances between subsystems and IP with corresponding pseudorapidity are presented in table [1].

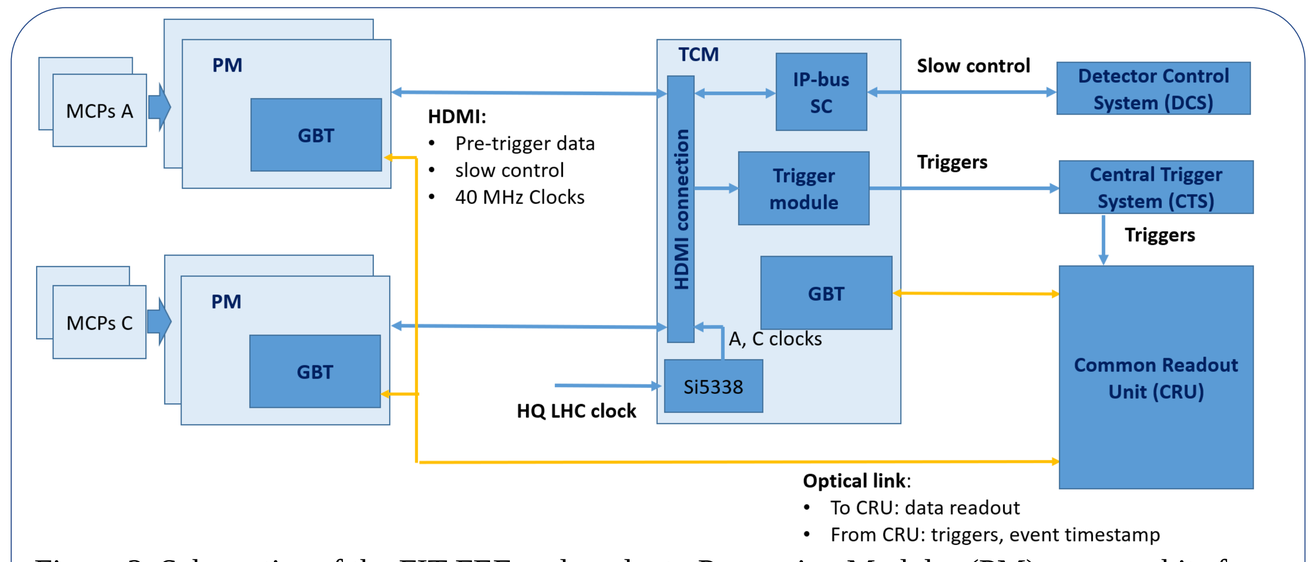
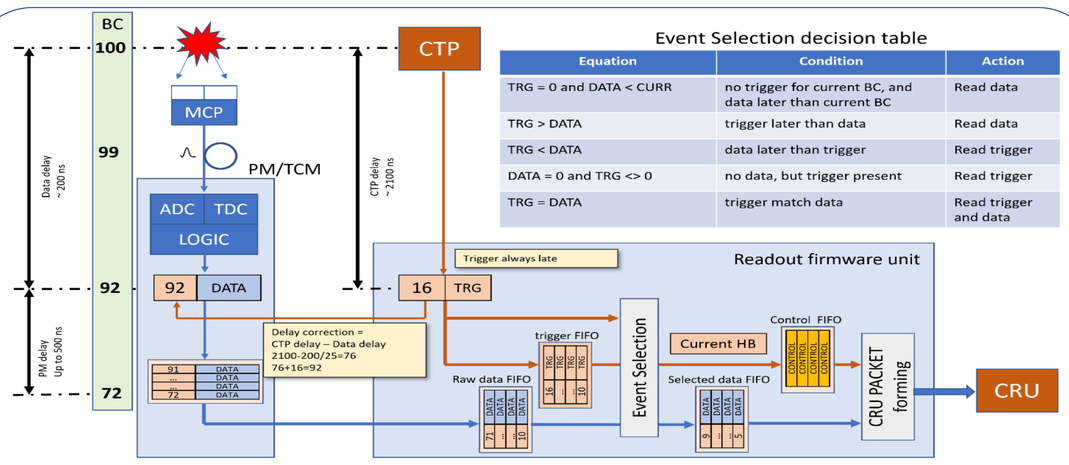


Figure 2. Schematics of the FIT FEE and readout.. Processing Modules (PM) measure hits from photosensors (MCP), send data to Common Readout Unit (CRU) [2] via GBT (GigaBit Transceiver) [3] and send pre-trigger data (charge sum and mean time) to Trigger and Clock Module (TCM) via HDMI cables. TCM module generates triggers with low-latency, and also sends data to CRU via GBT. TCM distribute reference clocks sourced from LHC HQ lock to PMs via HDMI. TCM is controlled via ethernet link and provide control of PMs via HDMI SPI (Serial Peripheral Interface) link [4, 5].



Event Selection decision table

Equation	Condition	Action
TRG = 0 and DATA < CURR	no trigger for current BC, and data later than current BC	Read data
TRG > DATA	trigger later than data	Read data
TRG < DATA	data later than trigger	Read trigger
DATA = 0 and TRG <> 0	no data, but trigger present	Read trigger
TRG = DATA	trigger match data	Read trigger and data

Figure 3 demonstrates the concept of event ID synchronization in the FIT FEE with the ALICE DAQ. On the scheme particle colliding happens at BC ID = 100. Due to distance between detector and interaction point and FEE tracts delays, FPGA latches data for hits delayed approximately by 200 ns or hits with BC ID = 92. At the same time CTP emits BC ID = 100, but due to cable delay ~2100 ns the FIT FEE receives from CTP the older BC ID = 16. Received BC ID from CTP is corrected with "BCID delay" value (2100ns – 200ns)/25 ns = 76 BCs for delay compensation. The correction value is measured during calibration procedure with an LHC beam for each PM/TCM unit independently. The corrected BC ID is coupled with measured hit data. After assignment timestamp to measured hit, calculation and data propagation delays makes no difference.

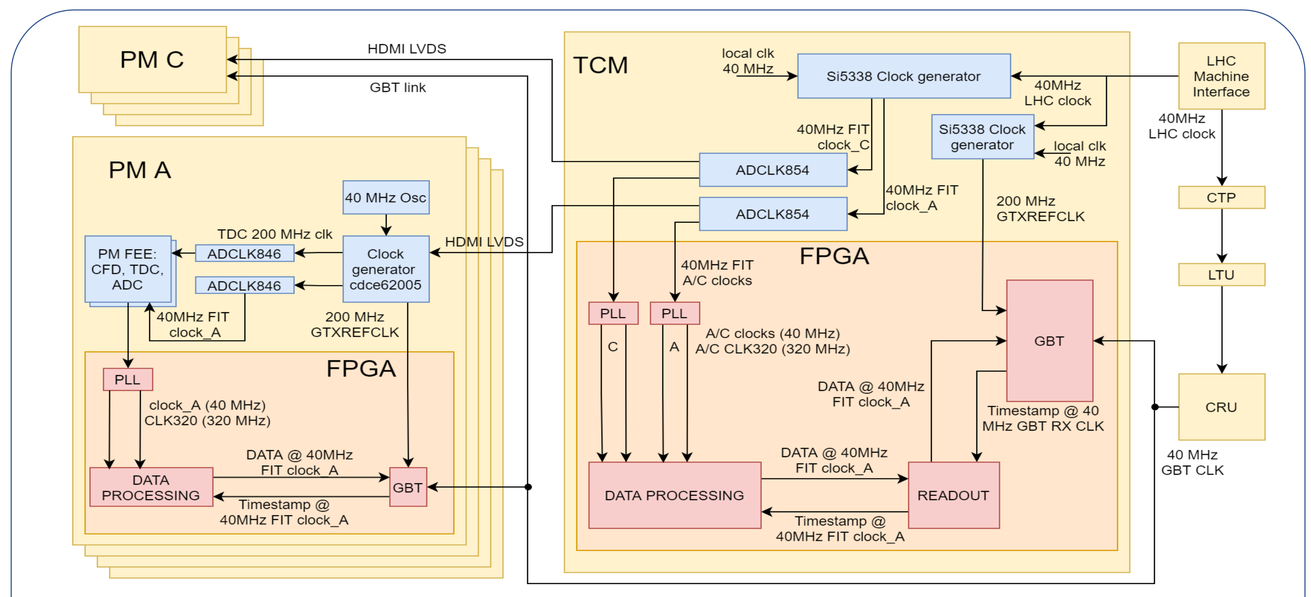


Figure 4 demonstrates the FIT FEE and readout clock distribution from the time synchronization point of view. The LHC HQ clock received from LHC Machine Interface via optical link is used as reference for clock generator Si5338 at TCM. Si5338 generates 40 MHz clocks for A and C FEE sides with controlled phase shift. Clock phase adjustment for A and C FEE sides allows to put signals to the middle of the ADC strobe and CFD gate, tuning mean time per side to zero. Generated clocks fanned out with ADCLK854 buffers and transmitted to PMs via HDMI cables in LVDS format. The clock is used as reference in PM for generation of 40 MHz "A/C clock" with 200 MHz TDC clocks in cdce62005 generator. The 320 MHz clock "CLK320" generated in FPGA PLL (phase-locked loop) and aligned to "A/C clock" is used for data processing in FPGA.

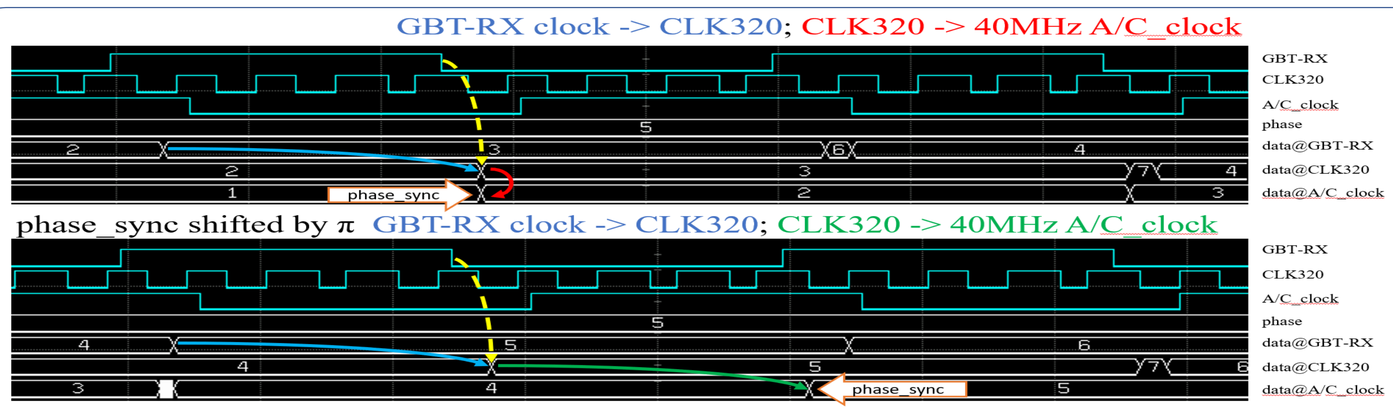


Figure 5. Using LHC HQ clock as source for FIT FEE allows to minimize phase drift between interaction time and event time measurements. FIT FEE receives event timestamps via GBT link by "GBT-RX" clock is synchronously but shifted to LHC HQ clock. Coupling timestamp to measured event needs moving data from "GBT-RX" to "A/C clock" domain with fixed latency. 320 MHz clock "CLK320" used for phase measurements between "GBT-RX" and "A/C clock" 40 MHz. Phase measurements allow latching GBT data with "CLK320" clock in the middle of the "GBT-RX" clock cycle excluding metastability state and data distortion even in the case of phase drift. GBT data by "CLK320" latched with 40 MHz "A/C clock" at fixed value of the phase counter "phase_sync". Transition of measured phase value through "phase_sync" value causes BC ID jump. **Top**: Signals diagram in the case of GBT data latency instability. GBT data transition from "GBT-TX" clock to "CLK320" (blue arrow) and from "CLK320" to "A/C clock" (red arrow) happens in the same clock cycle. The first transition follows the "GBT-RX" clock phase (dashed yellow arrow) and the second is tied to fixed phase "phase_sync" value. Jump of phase value by one affect to GBT data latency. **Bottom**: shifting of "phase_sync" value per π, that prevents BC ID jump with phase transition through "phase_sync" value. Shifting of "phase_sync" is applied to all PMs per single side in case the "A/C clock" edge concurs with the "GBT-RX" clock edge.

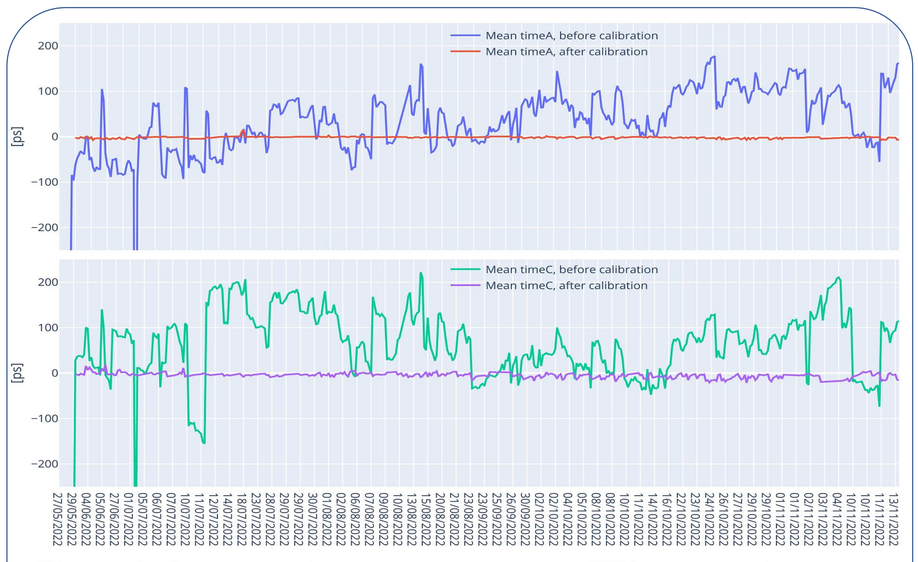


Figure 6. One of the important purpose of FT0 detector is to deliver high precision collision time for Time-Of-Flight detector. Mean FT0 collision time affected by season clock shift, time alignment is presented on the picture for all run periods LHC in Run 3 (May - Nov): side A – violet, top; side C – bottom, green. Time alignment deviation does not exceed 200ps during operation period before calibration. Online time offset calibration allow to correct time spectra position for each channel. Time alignment deviation does not exceed 20ps after calibration and is presented on the picture: side A – red, top; side C – bottom, purple.

[1] ALICE Collaboration, Maciej Slupecki, *Status of the Fast Interaction Trigger for ALICE Upgrade*, PoS ICHEP2020 (2021) 779. **[2]** F. Costa et al., The detector read-out in ALICE during Run 3 and 4, J. Phys. Conf. Ser. 898 (2017) 032011. **[3]** M. Barros Marin, Sophie Baron, S.S. Feger, P. Leitao, E.S. Lupu, C. Soos, P. Vichoudis, K. Wyllie, The GBT-FPGA core: features and challenges, JINST 10 (2015) 03, C03021. **[4]** ALICE Collaboration, D. Finogeev, *Readout system of the ALICE Fast Interaction Trigger*, JINST 15 (2020) 09, C09005 **[5]** ALICE Collaboration, D.A. Finogeev, Fully integrated digital readout for the new Fast Interaction Trigger for the ALICE upgrade, Nucl.Instrum.Meth.A 952 (2020) 161920.