Status of the Phase-2 Tracker Upgrade of the CMS experiment at the HL-LHC

Luigi Calligaris (SPRACE/UNESP) on behalf of the CMS Collaboration

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The Phase-2 tracker upgrade

○ Future HL-LHC upgrade ($5-7 \times 10^{34} \, \text{cm}^{-2}\text{s}^{-1}$)
  ○ Pile-up increase from 25 to 200 (x8)
    ○ Larger number of tracks → increase granularity
    ○ Larger hit & trigger rates → increase readout rates
    ○ More selective L1 trigger → Track information at L1
  ○ Lifetime radiation dose from 300 to 3000 fb$^{-1}$ (x10)
    ○ Improved radiation hardening of detectors
    ○ Easy to install, repair, replace
  ○ Reduce material budget

○ Entirely new Phase-2 tracker
  ○ Inner (IT) and outer (OT) tracker
  ○ Back-end systems
    ○ Read-out and control
    ○ Power supplies
    ○ OT L1 Track finder

LHC high pile-up test fill in 2016 ($<\text{PU}> = 80$)

- strip-strip OT: 31 M channels
- pixel-strip OT: 170 + 11 M channels
- IT: 2 B channels
Inner Tracker

- Big detector (1.95 billion channels, 4350 modules)
  - Challenge for read-out and calibration
- IT Geometry
  - Coverage extended to $|\eta| < 4.0$
  - 4 barrel layers, 8 + 4 endcap disks each side
  - 2-sensor modules (inner part) and 2x2-sensor modules (outer)
- Different sensor types are now under evaluation
  - (planar or 3D sensors) x (square or long pixels)
  - Compared to Phase-1, the pixels have $\frac{1}{6}$ area (2500 um²)
  - 3D sensors attractive for use in the innermost layers
    - Better SNR, radiation hardness, lower $V_{\text{bias}}$

![Graph showing data comparison](image)
Inner Tracker

○ Sensors directly bump-bonded to read-out chips
  ○ CROC based on the ATLAS/CMS project RD53
  ○ Highly integrated ASIC: “Analog island in digital sea”
  ○ Tests on RD53A and RD53B prototypes very encouraging
  ○ Final design of CROC ongoing, prototypes expected soon

○ IT modules use serial powering using a constant current src
  ○ Strings of up to 12 modules powered together
  ○ Power tapped as needed by each module through a shunt-LDO reg
  ○ Greatly reduces amount of Cu cables (material budget)
  ○ HV circuit is separate and fed in parallel

○ Modules communicate electrically via serial eLinks
  ○ eLinks connect to portcards located further away from beam
  ○ A portcard hosts 2 lpGBTs a DC-DC converter and optoelectronics
    ○ High speed optical serial links to the detector back-end
Outer Tracker

○ Coverage to $|\eta| < 2.4$

○ OT design driven by L1 track finder
  ○ pT-modules → select pairs of hits from hard tracks
  ○ These pairs of hits ("stubs") are read out at 40 MHz
  ○ The track finder reconstructs tracks and feed L1T

○ Two types of sensor modules at different radii
  ○ 2S: two microstrip sensors
    ○ Dimensions: 10 x 10 cm
    ○ Strip size: 5 cm x 90 um
  ○ PS: one macropixel + one microstrip sensor
    ○ Dimensions: 5 x 10 cm
    ○ Pixel size: 1.5 mm x 100 um
    ○ Strip size: 2.4 cm x 100 um
  ○ Pixel sensors improve z resolution and occupancy
  ○ Read-out is binary (no pulse height read-out)

○ Sensors manufactured by Hamamatsu Photonics K.K.
  ○ Pre-production runs started in July 2020
  ○ Begin of mass production expected 2021
Outer Tracker

- **2S strips read-out: CMS Binary Chip (CBC)**
  - 127 channels from upper + 127 from lower sensor
  - A correlation logic builds the “stubs”
  - 8 CBCs needed to read out each side of a sensor
  - Extensively tested in past years
  - Final mass-production will begin soon

- **PS strips read-out: Short Strip ASIC (SSA)**
  - 120 channels
  - 8 SSAs needed to read out each side of a sensor
  - Under development, testing prototypes

- **PS pixels read-out: Macro Pixel ASIC (MPA)**
  - 1888 channels
  - Contains the correlation logic to build stubs
  - 16 MPAs needed to read out a sensor
  - Under development, testing prototypes

- **PS and 2S: CMS Concentrator IC (CIC)**
  - De-randomizes data rate fluctuations from events
  - Forwards hits and stubs to the lpGBT

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A 2S front-end hybrid hosting 8 CBCs and a CIC

Schematic of the new revision of the CIC ASIC
Electronic system overview

- Outer tracker ASICS read out via serial eLinks
  - 6 links per sensor side @ 320 Mbps for 2S modules
  - 7 links per sensor side @ 320/640 Mbps for PS modules
  - 1 control link per sensor side @ 320 Mbps
- lpGBT located on-module (service/read-out hybrid)

- Inner tracker ASICS read out via 1.28 Gbps eLinks
  - High rate: 3 eLinks per read-out chip, 1 lpGBT/module
  - Low rate: data merging, 7 modules/lpGBT
  - 1 control link per module @ 160 Mbps
- lpGBT located on portcards

The lpGBT accomplishes all roles of module read-out, control and clocking using a single duplex optical link.
Track finding is computationally hard → need massive parallelization
- The read-out system is designed around the divide and conquer concept
- Division in space → 9 azimuthal “nonants”
  - nonants read out by groups of DTC cards
  - DTCs then send stubs to TFPs
- Division in time (“Time Multiplexing”) → 18 full copies of the TF system
  - Copies process events in turns (more time to complete the task)
  - event1→TFP1, event2→TFP2, …, event18→TFP18, event19→TFP1, ...
- High performance, low-latency processors
  - Large FPGAs used to run highly parallel reconstruction algorithms
Data, Trigger and Control cards

- A **high BW processor** to read out and control tracker modules
  - Up to **72 FE modules** via lpGBT links (5 or 10 Gbps)
  - **Builds** event fragments from data streamed from the FE ASICs
  - Forwards **hits to DAQ** and from there to the HLT (25 Gbps optical)
  - Sends **timing, trigger and control** data to FE modules
  - Performs detector calibration using on-board resources
  - (OT) Performs stub conversion from module-local to global coordinates
  - (OT) Routes stubs to their assigned Track Finders (25 Gbps optical)

- Total of 216 (OT) + 28 (IT) DTCs in the system

- Large power & cooling needs → ATCA standard

- **The Serenity board** will be used to fulfill the OT DTC role
  - Need to process up to 120 serial high-speed optical links
    - Xilinx Virtex UltraScale+, either 1 x VU13P or 2 x VU7P
    - Firefly high density transceivers (12 ch @ 28 Gbps)
  - SoC (x86_64 or ZYNQ module) running CentOS Linux
    - Used for calibration, configuration & system control

1 x VU13P design  2 x VU7P design

Serenity prototype with 2 x KU15P
Track Finder Processors

- Different algorithms in FPGA explored in the past:
  - Tracklet seeding + iterative road search + linear fitter ("Tracklet")
  - 2D Hough transform + Kálmán filter ("TMTT")

- Current "Hybrid" algorithm merges the two approaches
  - Tracklet seeds are created from pairs of stubs in pairs of layers
  - Search for matching stubs in the next layers, then merge duplicate tracks
  - Candidate tracks pass through a Kálmán filter → track parameter fit
  - Up to 300 tracks/evt = 12 billion tracks/s, with < 4 us latency

- Total of 162 track finder processor cards in the system

- **Apollo board** targets the TFP and IT DTC role → large FPGAs with lots of resources
  - Xilinx Virtex UltraScale+, either 2x VU9P or 1x VU13P
  - Firefly high density transceivers (12 ch @ 28 Gbps)
  - 2-piece board: Command Module (TF FPGA/Fireflies) and Service Module (carrier)
    - Apollo, similarly to Serenity, hosts an SoC tasked with board management duties
    - ATCA standard: high electrical power, cooling & reliability
Testing of the OT modules

○ As OT modules are produced, they will need to be tested
  ○ System based of the FC7 AMC card (Kintex7 420T)
    ○ d19c firmware in FPGA
    ○ Phase2 Acquisition Control Framework in control PC
    ○ Communication via IPBus/UDP protocol
  ○ Automated testing of module components using a dedicated crate

○ The framework is also used to test full modules at test beams
  ○ Optical read-out and control, like in the final experimental setup

○ Wide expertise gained in the development of these testing tools
  ○ A test bed for the development of the DTC firmware
Summary

- HL-LHC Upgrade
  - Challenge for sensors, readout, trigger and detector materials

- CMS Phase-2 Upgrade
  - Inner (pixel) + outer (strip/pixel) trackers
  - Both under intense research & development activities
  - Some components to begin mass-production and assembly very soon
    - Installation and commissioning of new tracker → Long Shutdown 3 of LHC

- L1 Track finding
  - Outer tracker back-end will reconstruct tracks for the L1 trigger
  - Very large system running reconstruction algorithms on FPGAs
Thanks! Спасибо! :)}