mPSD readout system at mCBM experiment

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The Projectile Spectator Detector (PSD), a sampling lead/scintillator forward hadron calorimeter with transverse and longitudinal segmentation and with MPPCs photodetectors, will be used at the Compressed Baryonic Matter (CBM) experiment at FAIR to measure the centrality and orientation of the reaction plane in nucleus-nucleus collisions. After conversion in the FEE (Front End Electronics), signals from the MPPCs are digitized with LMT9011 ADCs with 14 bit digitization and up to 125 Msps rate which has been developed for the ECAL of the PANDA experiment at FAIR. The Kintex 7 FPGA is used for signal processing and data collection. The trigger-less readout is based on the GBT-FPGA.

Components related to the signal chain (MPPCs, cable runs, ADC interface) and readout firmware have been tested and confirmed to be operational during beam tests runs at mCBM@SIS18 at the end of 2019 and beginning of 2020. Overview of electronic components for the full-size PSD calorimeter are shown, as well as the first results from mCBM beam test at March 2020

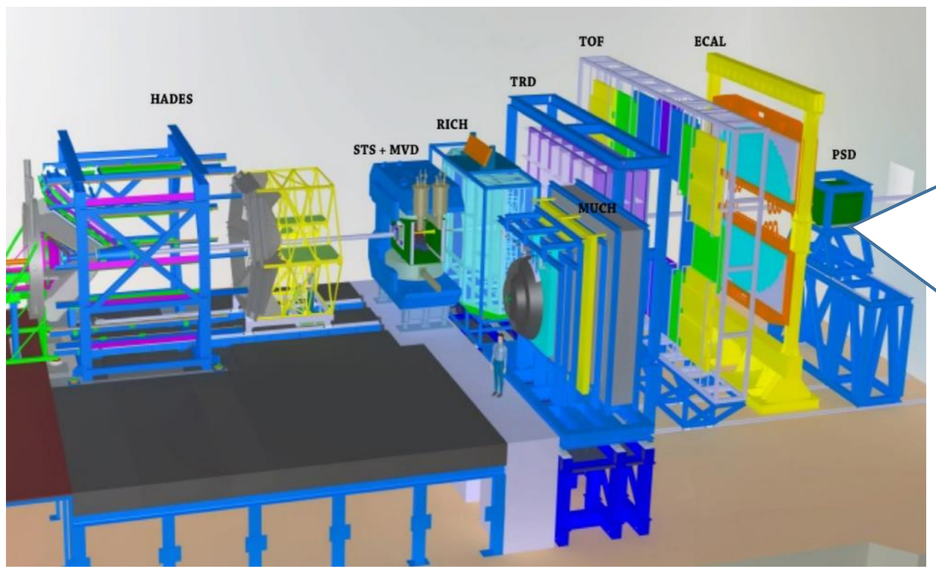


Fig. 1 CBM will explore strongly interacting matter at highest net-baryon densities by investigating nucleus-nucleus collisions in fixed-target mode with extracted beams from the SIS-100.

- high-rate capability of up to 10^7 interactions per second
- CBM will employ fast and radiation-hard detectors and readout electronics
- free-streaming data acquisition system
- self-triggered front-end electronics

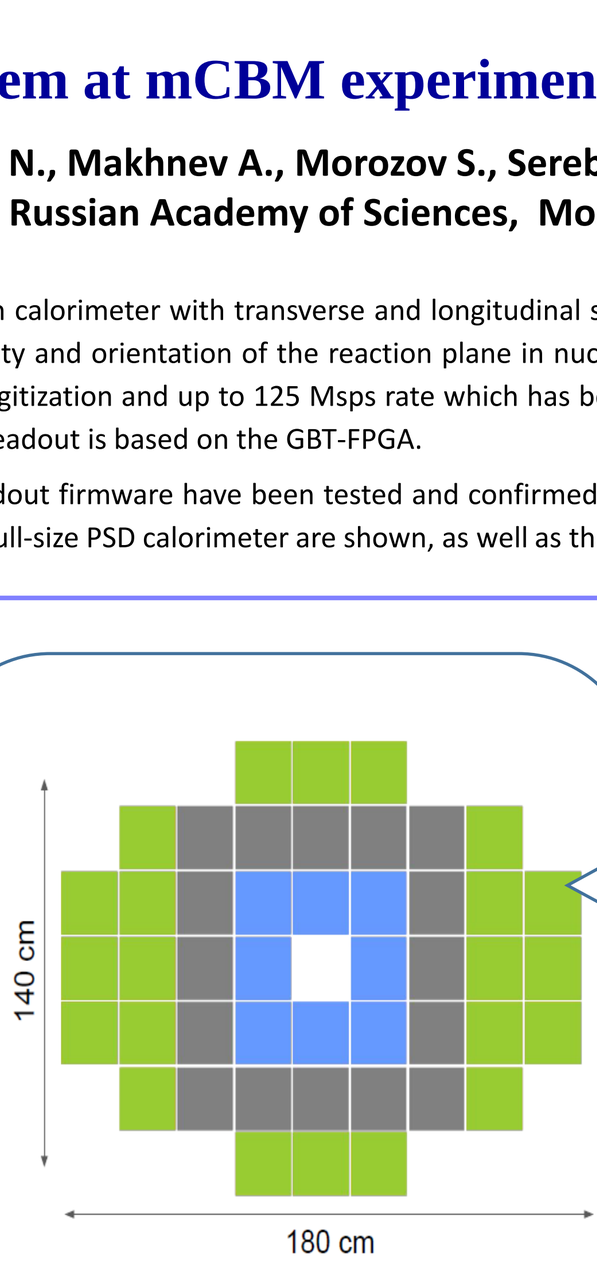


Fig. 2 46 modules; 200x200mm^2 ; Beam hole 20x20 cm^2; Total weight – 22t All modules already constructed by the end of 2017

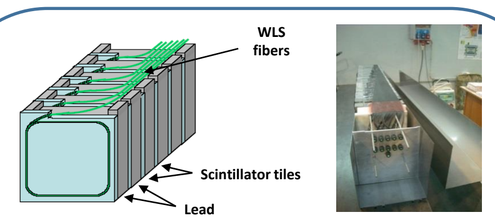
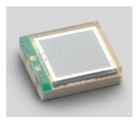


Fig. 3

- Module transverse size 200x200mm^2 .
- Longitudinal structure: 60 Pb/Scint tiles layers: (Pb(16mm), Scint(4mm) grouped in 10 sections.
- Total length is 5.6 λ_{int}.
- Weight of each module 500 kg.
- Light collection – by WLS fibers from 6 sequentially placed scintillator tiles in one section to one optical connector at the end of module.
- Light readout: 10 MPPC (3x3mm^2) per module.
- Readout electronics: sampling ADC.



Hamamatsu *S12572-010P*
Sensitive area 3x3 mm^2
Number of pixels 90 000
Nominal gain 1x10^5
Pixel recovery time 10 ns

System architecture

- Electronics consist out of two major parts:
  - Radiation-hard “Detector side” (mounted directly on PSD)
  - Radiation-sensitive “Readout rack”
- Detector side includes:
  - One FEE board per each module
- Readout rack includes:
  - 7-8 Readout modules
  - One service board
- MPPCs are connected directly to the digitizer via coaxial 5 mm 50 Ohm cables

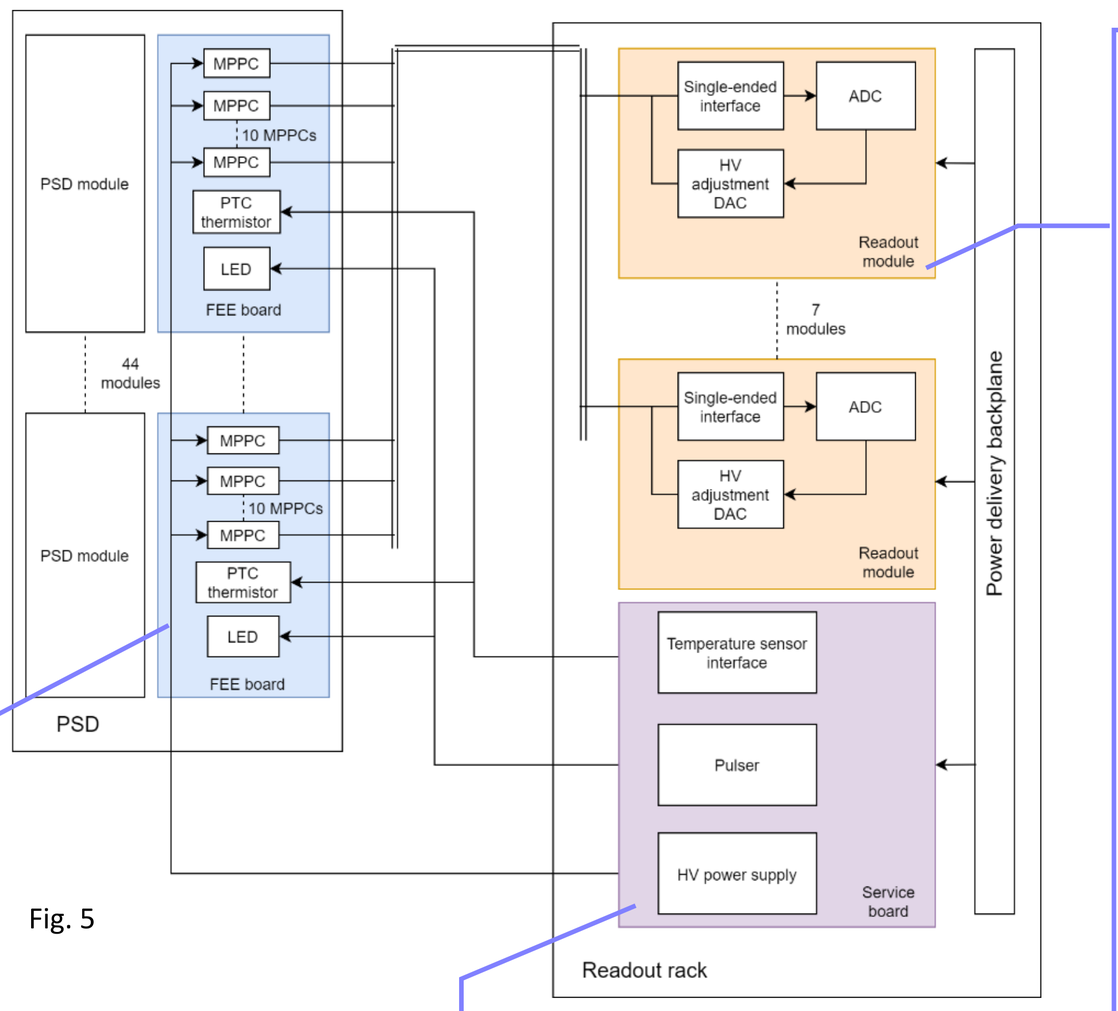


Fig. 5

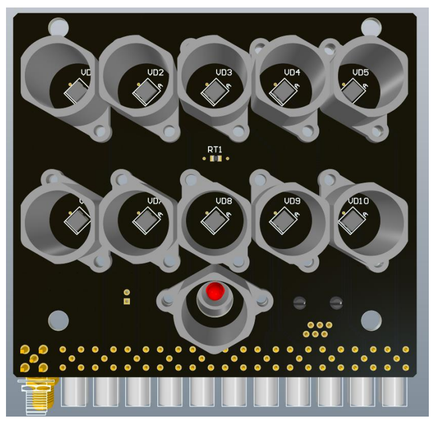
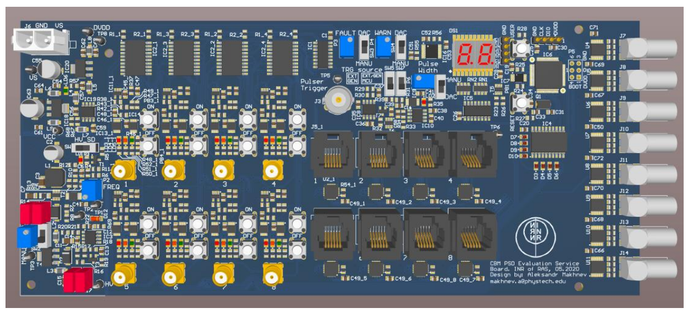


Fig. 4 FEE board

- Hosts:
  - 10 MPPCs
  - Calibration LED
  - Temperature sensor
  - Light protection hardware
- Mounted directly onto a PSD module
- Provides direct signal feed from the MPPCs
- Board is designed and is in production

Fig. 6 Service board

- Hosts:
  - High voltage power supply
  - MPPC current monitor and protection
  - Temperature sensor interface
  - LED calibration pulse generator
- Slow control client MCU
- An evaluation version of the board is developed and manufactured



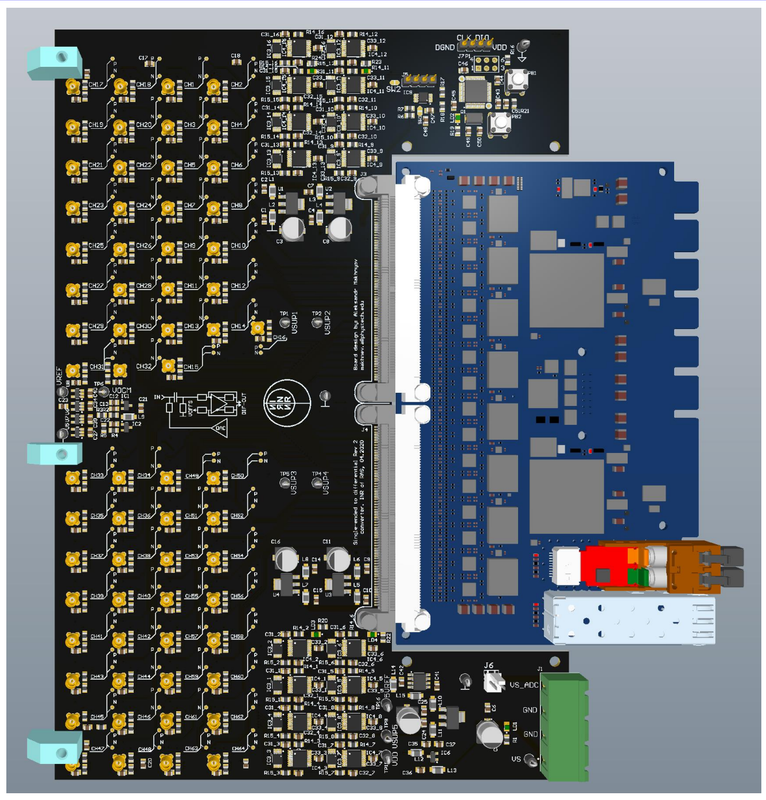


Fig. 7 Readout module

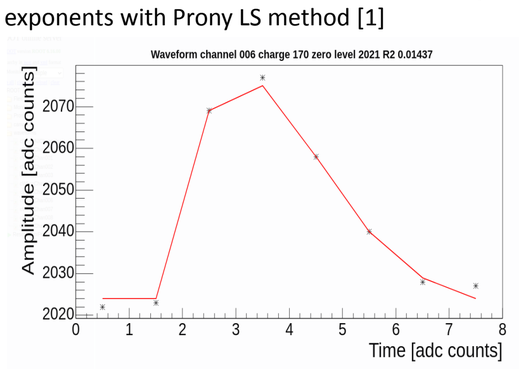
- Single-ended ADC interface module: adjustable input and output zero level, 1:1 conversion ratio
- ADC64 board
  - LTM9011 ADC
    - 125Msps / 80Msps (used now)
    - 14-bit digitization
    - Selectable Input Ranges: **1VP-P (used)** to 2VP-P
  - Two FPGA Kintex 7
    - 32 channels per one FPGA
    - Separated optical link for each FPGA
    - Signal processing on the fly
  - Readout rate
    - 3.2 Gbit/s (GBT 80bit@40MHz)
    - Top limit: 3.2 Gbit/s / 32 channels / 1 MHz readout rate = 100bit/hit (80bit used now)
- High voltage adjustment circuit via per-channel common-mode compensation

The prototype of PSD detector with readout system was implemented and tested in the first high rate heavy ion interactions at mCBM@SIS18 at GSI, Darmstadt in March 2020. One module of PSD (mPSD) was installed at mCBM experiment which includes prototypes of all detectors of CBM@FAIR experiment as MVD, STS, MUCH, TRD, TOF, RICH and ECAL. The mPSD setup included all crucial parts of PSD readout system: MPPCs, ADC interface board, ADC board and firmware for ADC board. Data from mPSD as well as other subsystems was collected with common mCBM DAQ.

One of the major feature of ADC board is possibility to process signals on-the-fly with FPGA. Fitting the signals waveforms will allow to improve time and amplitude resolution and perform pile-up selection [1]. Typical waveform measured with 80 MHz digitization is shown in the figure 8. To recognize pile-ups at expected high load rate up to 1MHz at CBM experiment, digitization rate of ADC will be increased to 120MHz with firmware upgrade.

Components related to the signal chain as well as firmware and software parts have been tested and confirmed to be operational during beam test runs at mCBM@SIS18 at the end of 2019 and beginning of 2020. [2] Most components needed for assembly of the full-size PSD’s electronics architecture are either designed or undergoing manufacturing.

Fig. 8 Example of mPSD signal waveform measured during beam test at mCBM@SIS18 in March 2020. Black dots – waveform measured by ADC, red line – is based on waveform fit by two exponents with Prony LS method [1]



[1] Application of the Prony least squares method for fitting signal waveforms measured by sampling ADC. N.Karpushkin et al. AIP Conf. Proc. v2163, n1, 2019 DOI: 10.1063/1.5130092
[2] The readout system of the CBM Projectile Spectator Detector at FAIR. D.Finogeev et al. JINST 15 (2020) no.09, C09015 DOI: 10.1088/1748-0221/15/09/C09015