Implementation of the deconvolution method for signal peak detection in read-out ASIC

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Introduction

Usually analog or digital peak detector are used to determine the impulse maximum in analog channel. One of the problems of signal processing in an analog channel is signal superimposition at high channel signal rate, resulting in a loss of amplitude information. To resolve the issue, it is proposed to use the deconvolution method, which allows to separate the superimposed signals and determine their amplitudes.

Deconvolution method

Delta impulse of detector current is converted by an analog channel having a transfer function H(s). The output signal is digitized by an ADC, producing sampling sequence. Further the sampling sequence processed by deconvolution digital filter having transfer function W(z). If W(z) = 1/H(s), then the deconvolution filter output will contain several non-zero samples with values proportional to the input signal amplitude. The filter coefficients are calculated from the inverted transfer function (1/H(s)) of the analog channel.

One non-zero sample at the output of the deconvolution filter is provided when the input signal peak time is synchronous with the ADC sample. If the peak time of the input signal is asynchronous with the ADC sample, the output of the deconvolution filter will have a two non-zero samples. Figure below shows example of synchronous and asynchronous cases. For the asynchronous case, the peak value of the signal is sum of the non-zero samples at the filter output.

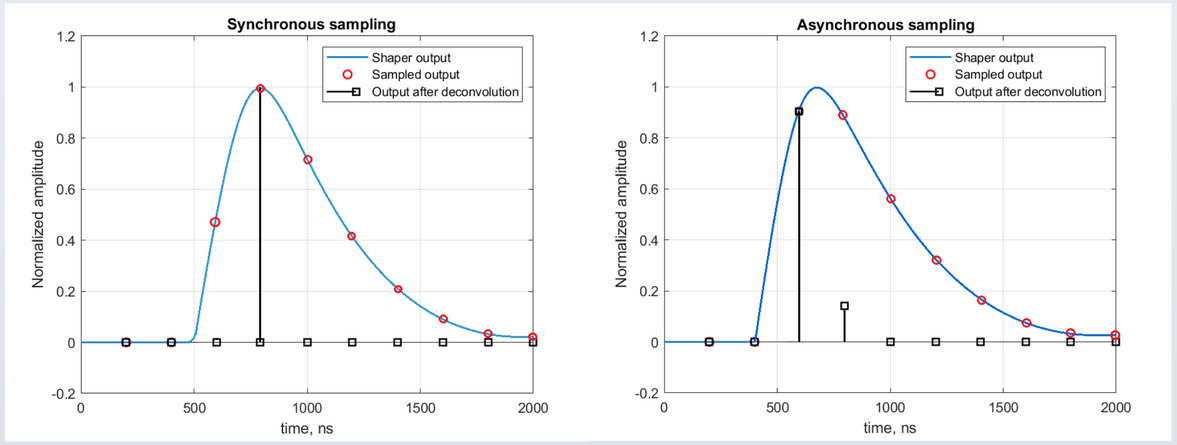
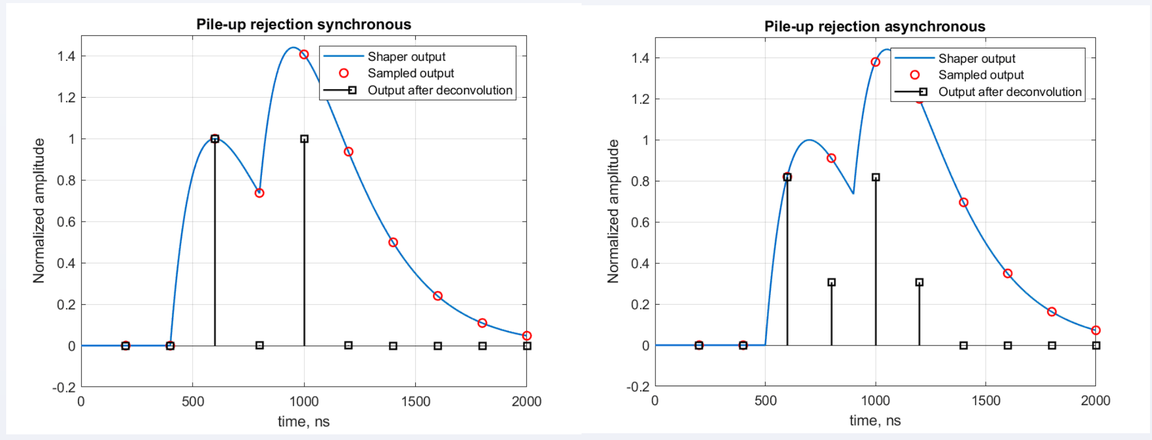


Figure below shows the error of peak determination versus the amplitude (% from the maximum ADC output value). It shows errors for digital deconvolution filter (red line) and digital peak detector (blue line) for analog channel featuring 2-order shaper at 250 ns time constant and 10-bit 25 MSPS ADC.

When two pulses are superimposed, there are two groups of non-zero samples at the deconvolution filter output. An example of the deconvolution output is shown in the figure further. In the implemented version of the deconvolution filter has been realized with a 4-samples window to separate two signals. The window width determines the resolution time of impulses separation.

The error of input signal peak determination is 9 LSB at the maximum amplitude. An error decrease of the deconvolution method at low amplitudes is limited by the ADC data width, which decreases the accuracy of signal waveform determination. It increases the error against theoretically one.

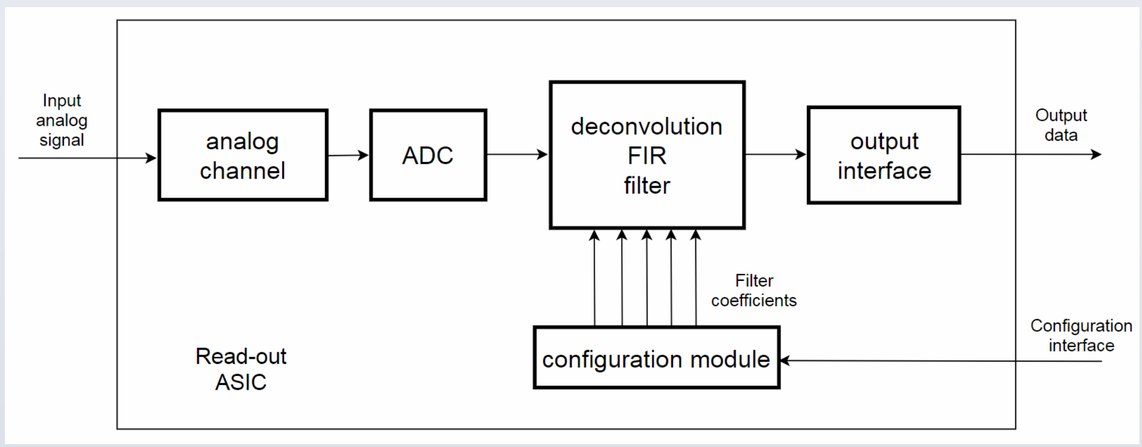
Peak detector has a dead time defined by a shaper fall time. If this condition is not met, the shaper output will contain the sum of the input signal and the falling edge of the previous one. In the case the calculated amplitude will be wrong. This limits the maximum channel signal rate.



Analog channel with the 2-order shaper at 250 ns time constant has the output fall times about 700 ns. The fall time defines the dead time of the peak detector. The deconvolution filter allows to reduce the minimum interval between pulses with their correct separation. Using of the 4 samples resolution deconvolution method at 25 MSPS ADC provides 100 ns dead time, which allows to increase the channel signal rate up to 7 times.

Implementing a deconvolution filter in a read-out ASIC

Deconvolution filter was implemented in a read-out ASIC for a GEM detectors. Figure below shows a fragment of the read-out chip structure with the deconvolution filter.



The signal passes through an analog channel. Then it is converted by an ADC into a sequence of samples at a frequency of 20-30 MHz and is processed by a 4-order deconvolution FIR filter. Next, FIR filter output samples sequence is read out over a high speed serial interface at 320 MHz.

In order to tune the filter to the channel characteristics and the input detector capacitance, the filter coefficients are not fixed and loaded by a serial configuration (slow control) interface.

In this implementation of the read-out ASIC peak value of input impulse is calculated outside the ASIC.

Deconvolution filter was developed for the UMC CMOS MMRF 180 nm process. The filter block has area of 645,4x207,6 sq. um. Its power dissipation is about 7,28 mW at 80 MHz (filter clock frequency).

Conclusion

The implementation of the deconvolution method for signal peak detection in read-out ASIC has been considered. The designed deconvolution filter allows to separate and restore the amplitudes of superimposed signals in case of a time interval between peaks is at least 4 ADC samples. This increases the channel signal rate up to 7 times for a 2-order shaper at a 250 ns time constant used and 25 MSPS ADC sampling rate.

Acknowledgments

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