Read-out electronics for LEGEND-200 experiment

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1. The LEGEND Project

LEGEND

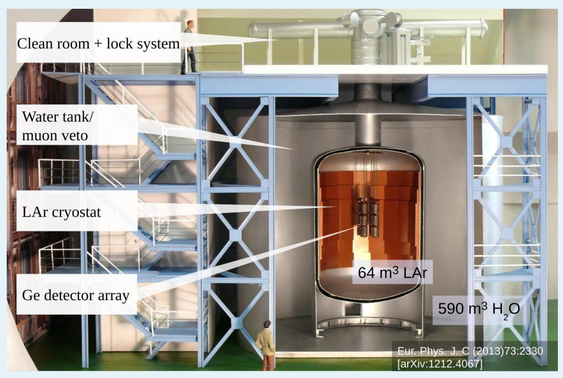
Large Enriched Germanium Experiment for Neutrinoless ββ Decay

LEGEND [1] is an experimental program to search for the neutrinoless double beta ($0\nu\beta\beta$) decay of ^{76}Ge aiming to reach a discovery potential at half-life beyond 10^{28} yr

- based on existing resources and technologies from GERDA [2] and MAJORANA [3] experiments, contributions from other groups and experiments
- first phase (LEGEND-200) with 200 kg of High Purity Germanium (HPGe) detectors enriched in ^{76}Ge, subsequent stage with 1000 kg (LEGEND-1000)

2. LEGEND-200 Experiment

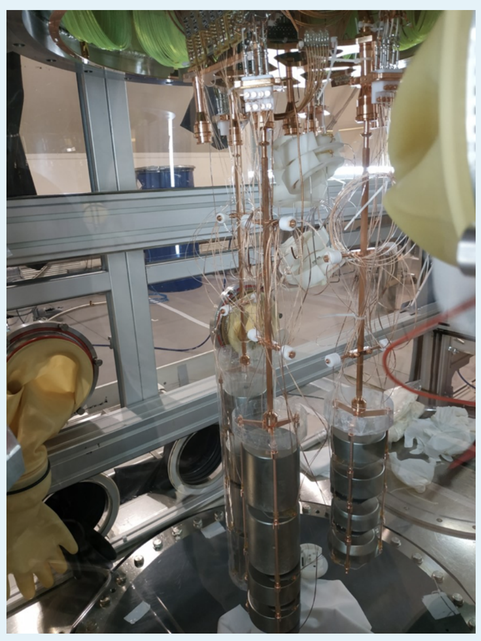
The first stage of the project LEGEND-200 already started:



- 200 kg of HPGe detectors in the GERDA [2] infrastructure at Gran Sasso Laboratory, operated directly in Liquid Argon (LAr)
- energy resolution of 2.5 keV (FWHM) in the region of $0\nu\beta\beta$ decay of ^{76}Ge (2039 keV)
- reduced background, goal of 0.6 cts/(FWHM·ton·yr)
- **data taking foreseen in 2021!**

Status of LEGEND-200

- GERDA infrastructure now operated by LEGEND from February 2020 with installation of the first setup
- **Electronics chain**: demonstrated with 20 channels in the first setup
- **New Detectors**: production of 155 kg of Inverted Coaxial HPGe in progress
- **New Active LAr veto**: production of fiber shroud and SiPMs in progress
- **Monte Carlo Simulations and Analysis Software** in preparation



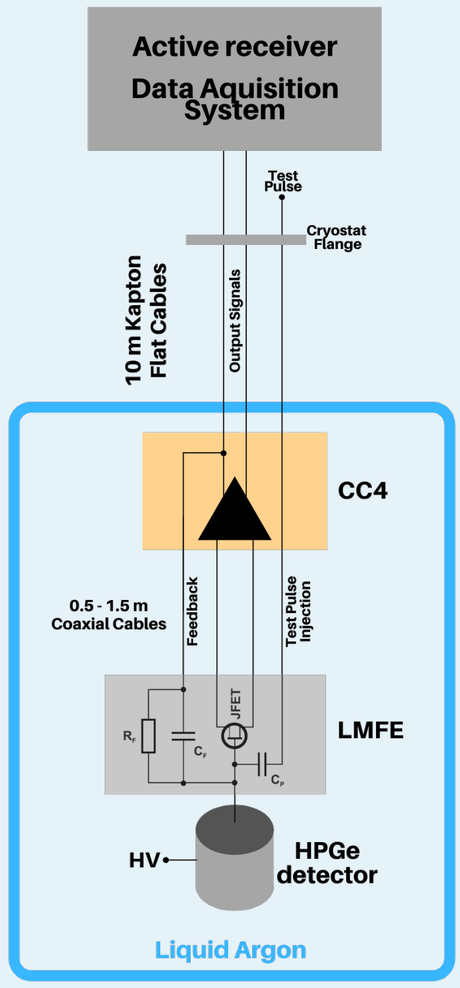
3. Read-out Electronics Design in LEGEND-200

The peculiar situation of HPGe detectors deployed directly in LAr and the requirement of very low radioactive background, introduces several constraints on the design of the read-out.

The LEGEND-200 read-out electronics consists in a Charge Sensitive Amplifier separated in 2 stages in order to both improve performance and reduce background:

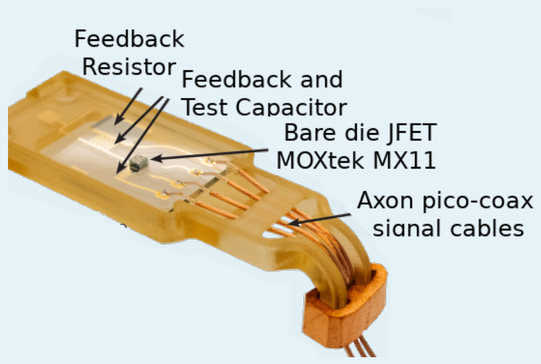
- **first stage** based on the MAJORANA Low-Mass Front End (LMFE) (see section 4)
- **main amplifier stage** based on the GERDA design (see section 5)

In addition, the system consists of a novel active, room-temperature, receiver and data acquisition system to read out up to 200 detectors



4. First Stage: Low-Mass Front End (LMFE)

The Low-Mass Front End (LMFE) is placed in the proximity of the Ge detector where very stringent radiopurity constraints have to be met; it has been designed and assembled in the Lawrence Berkeley National Laboratory

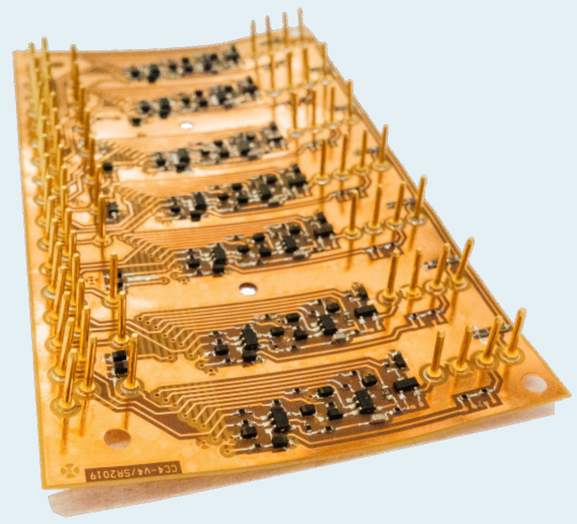


- **substrate**: Suprasil 500 μm thick
- **traces** in thin, sputtered, Ti/Au
- **JFET**: bare-die Moxtek MX-11, attached to substrate with conductive silver epoxy and Al wire bonds
- **feedback resistor**: sputtered aGe thin film with ~ 1 GΩ at 87 K
- **feedback and pulser capacitance** stray capacitance between traces

5. Main Preamplifier Stage: CC4

The CC4 design is based on GERDA design and is placed 40 - 140 cm above the HPGe detector, radiopurity requirements are less stringent w.r.t. LMFE

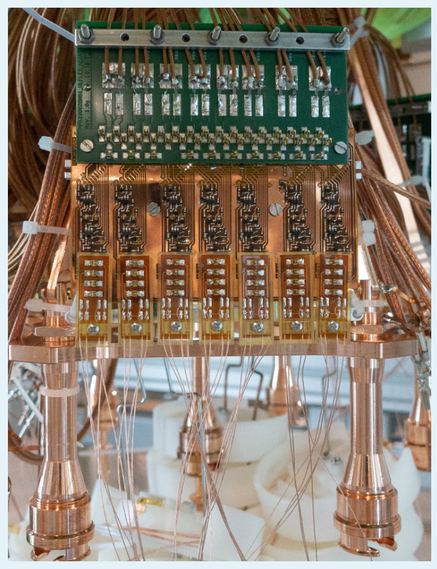
- **low-mass Kapton** circuit board
- footprint **SMD components**
- **differential signal output** to reduce potential noise and cross talk while driving 10 m long cable
- 7 read-out channels each CC4, up to 30 CC4 in LEGEND-200
- **axon pico-coax cables** to connect the LMFE with a strain relief provided by clamp made from electro-formed copper



6. Integration with HPGe detectors

The LEGEND-200 detector array utilizes a ultra-low-background mechanical design:

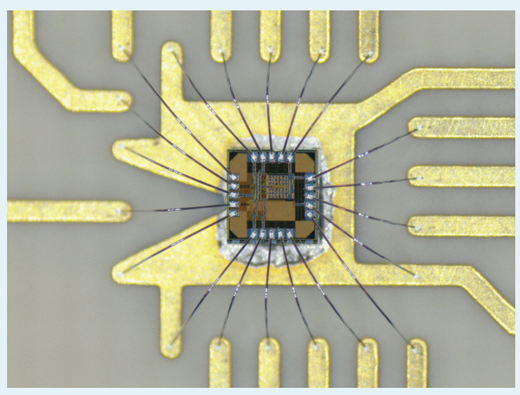
- clean structural materials: underground electro-formed copper, silicon detector plates and polyethylene naphthalate (PEN)
- detectors are connected to the read-out and high voltage via aluminum wire bonds
- modular electronics mount using clean engineering plastics (polyetherimide - PEI / ULTEM)



7. Outlook: Read-out Electronics for LEGEND-1000

For LEGEND-1000, the background coming from the signal read-out electronics has to be further reduced with a new radiopure solution

- the collaboration is actively developing novel, ASIC-based, signal read-out electronics
- that can integrate all the components into a single, low-mass and low-background silicon chip
- work to reduce the number of signal cables and find new structural materials and mechanical designs



LBNL-developed ASIC chip

References

[1] LEGEND Collaboration, AIP Conf. Proc. 1894, 020027 (2017)

[2] GERDA Collaboration, Science 365, 6460 (2019)

[3] MAJORANA Collaboration, Phys. Rev. C 100, 025501 (2019)