The Burn-in testing of advanced custom low-voltage power supply components within ATLAS TileCAL testing facilities.

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on behalf of the ATLAS collaboration

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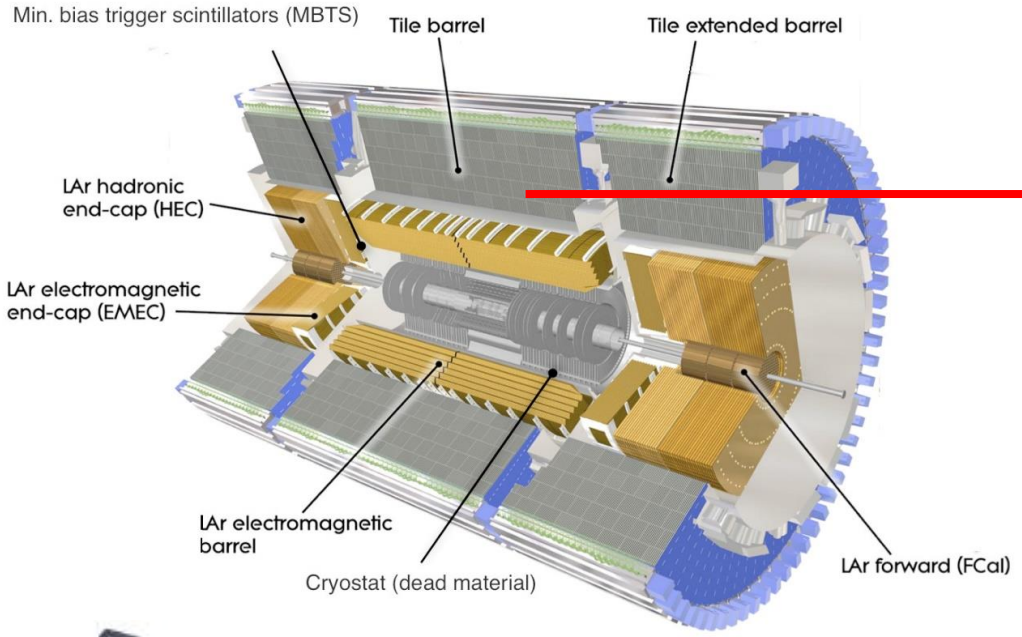
The 5th International conference on particle physics and astrophysics.

Talk Outline

- The LVPS in context.
- The LVPS brick.
- Motivation for the LVPS brick upgrade.
- What is Burn-in testing.
- LVPS Brick Burn-in station.
- The custom Burn-in station PCB’s.
- The Burn-in test station chassis.
- The Burn-in test station cooling system.
- The Burn-in test station test sequence.
- Summary

The LVPS brick in context



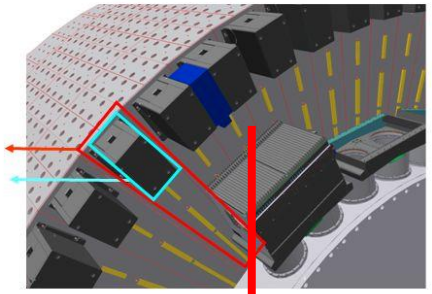
Tile Calorimeter

Module

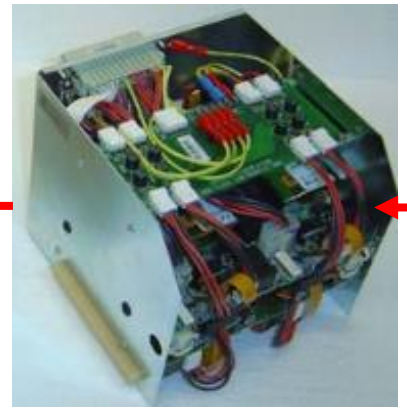
Electronics drawer

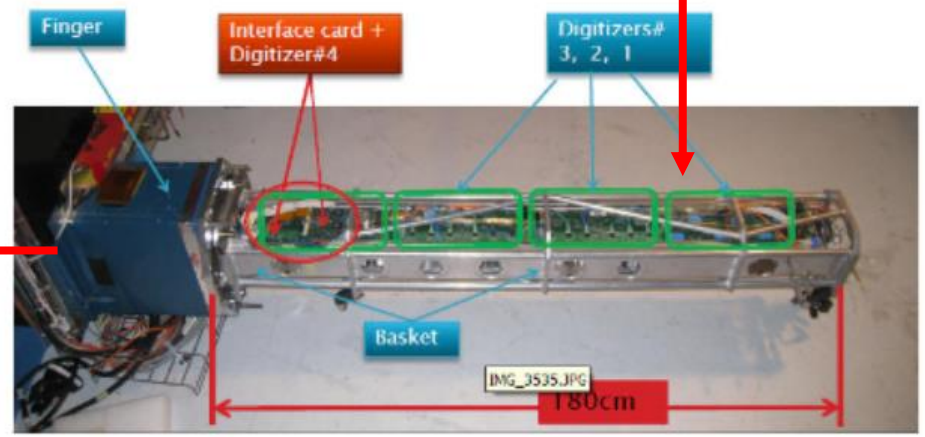
Finger

Module



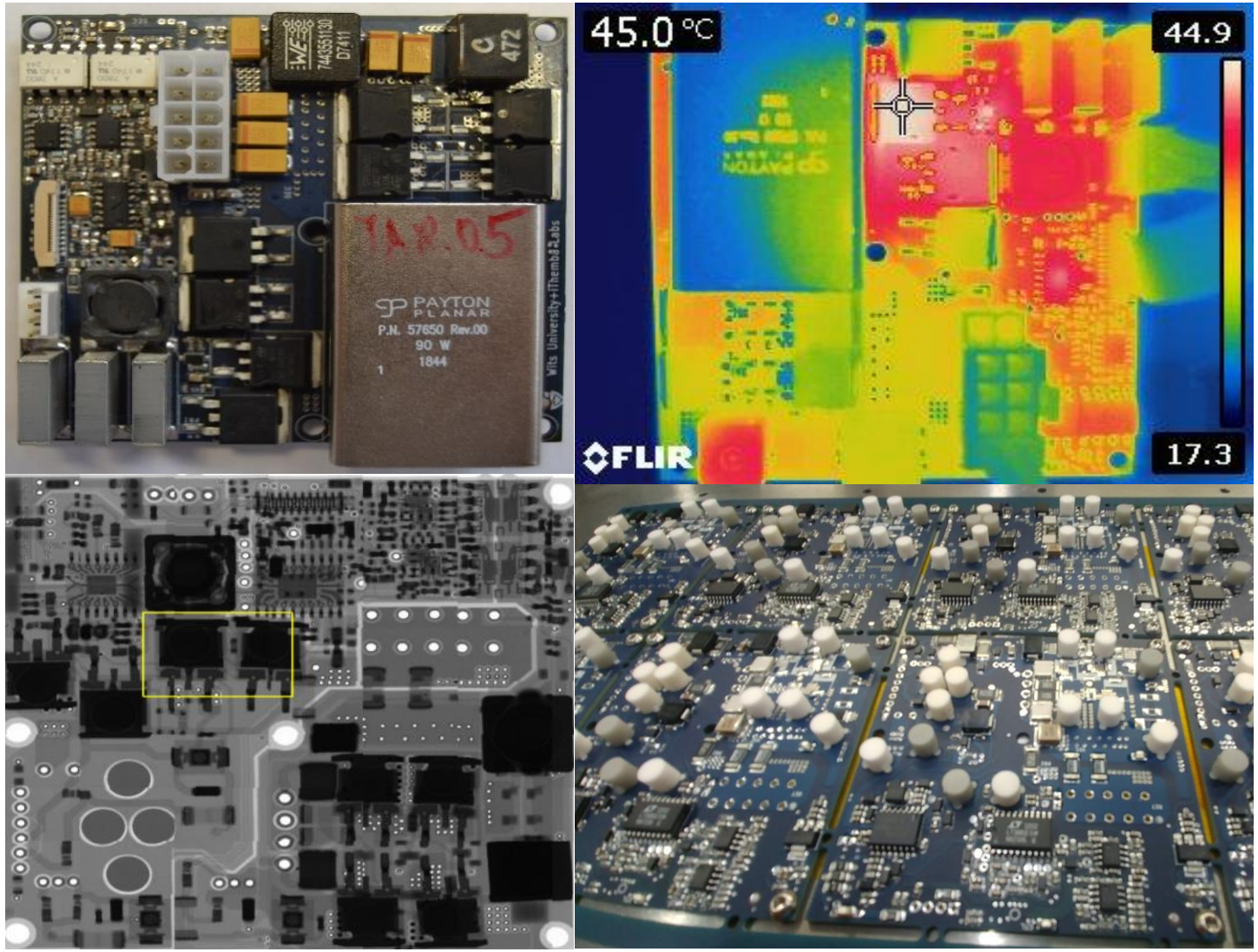
Tilecal: one barrel (6m), endcaps (3m).
- 256 drawers with front end electronics.
- 256 power supplies, 300W each.





The LVPS Brick

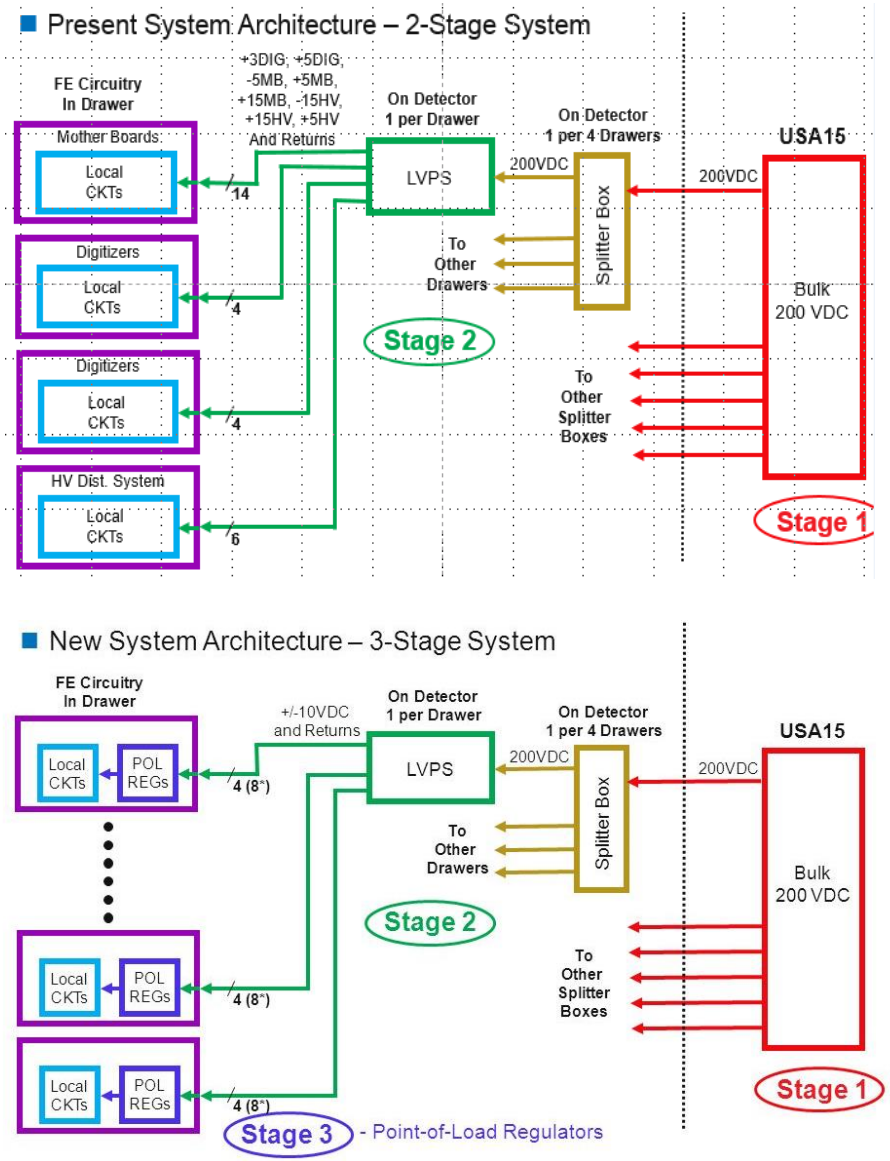
- Topology: A transformer coupled buck converter.
- Function: To convert bulk 200VDC power to the 10VDC which Is distributed to point-of-load regulators located on the Front-end electronics.
- V8.4.2: Current iteration going to Functional design review.
- Identical footprint to bricks currently installed within ATLAS allowing for drop-in replacement.



Version 8.4.2 Hybrid Brick produced within South Africa

Motivation for LVPS brick upgrade

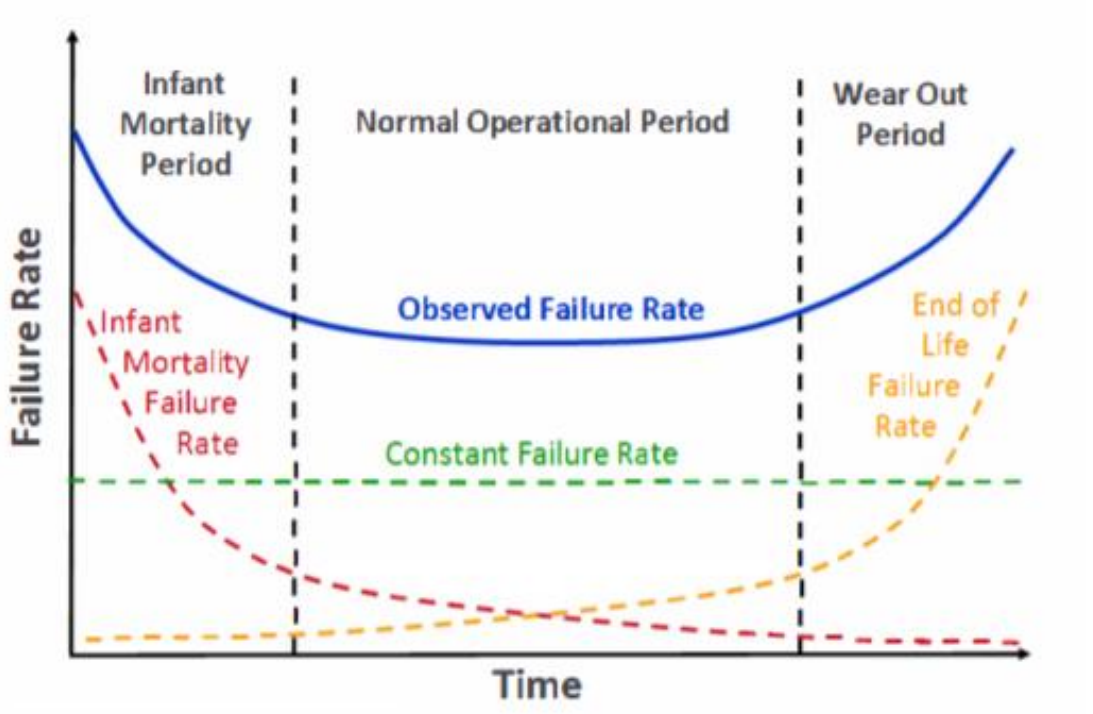
- The main TileCAL upgrade pertains to the Front-End (FE) electronics: all data sent out is now digital, trigger signals are no longer analogue.
- Upgrade from a 2-stage to 3-stage power distribution system to accommodate the FE upgrades.
- Emphasis is placed on the reliability of the particle detector and by extension all of the subsystems and electronics therein
- LVPS's represent a single point failure in the readout system. – loss of data from a particular module.
- Limited access to LVPS on the order of once per year.



Burn-in Testing

- A form of accelerated aging of electronic components.
- Purpose: To improve the reliability of the LVPS bricks.
- Method: The operation of the LVPS bricks at a higher load and operating temperature should cause the components to fail immediately within the Burn-in station as opposed to prematurely within ATLAS.
- Failed components can be repaired before installation within ATLAS.
- Previous Burn-in testing contributed to an annual failure rate of the V7.5 on the order of 2 per year, ~0.1% of population.
- Taking place at the University of the Witwatersrand (WITS) and the University of Texas at Arlington (UTA).

Bathtub curve of electronics failure rate



KEMET Tantalum capacitor
Highest failure rate (FIT = 288) before voltage de-rating
Current V7.5 Bricks within ATLAS experience ~ 2 failures per year which constitutes ~ 0,1 % of the total population.

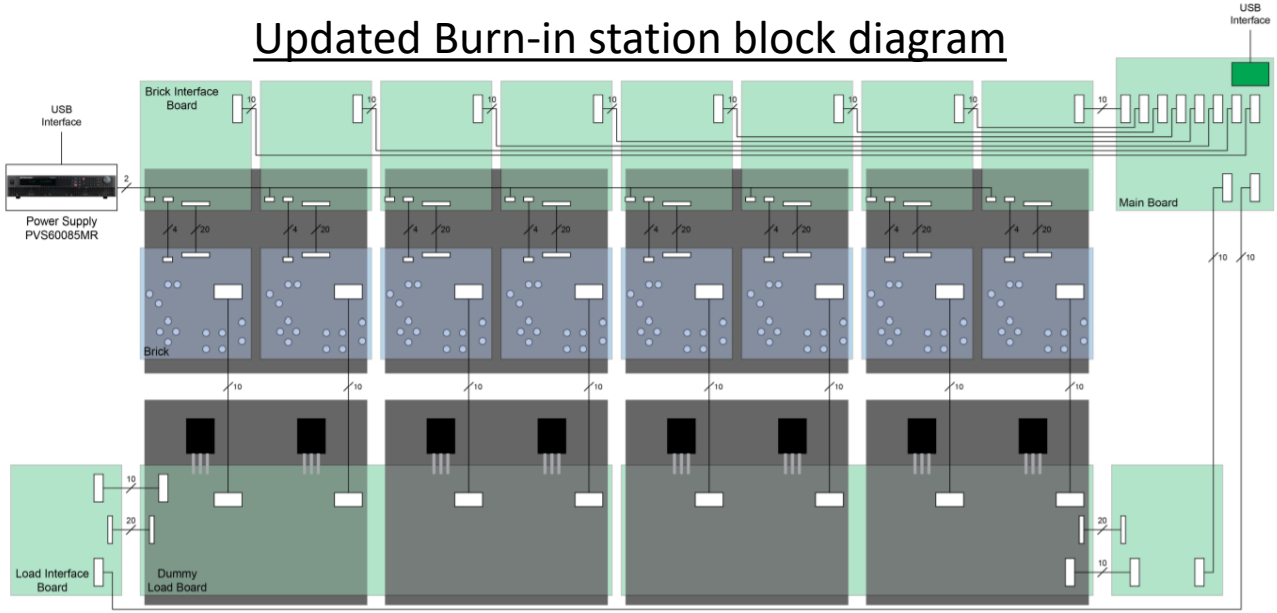
LVPS Brick Burn-in station

Composed of:

- Chassis
- Cooling system
- Custom PCB's: Mainboard, Interface-boards and Dummy-load boards
- Power supply (200V)
- LabVIEW control program
- Desktop PC

- Utilizes a legacy design as a framework.
- A total of four will produced, 2 by WITS and 2 by UTA.
- The test stations will be required to test approximately 2048 bricks starting with the testing of 200 bricks as part of pre-production in mid 2021.

Updated Burn-in station block diagram



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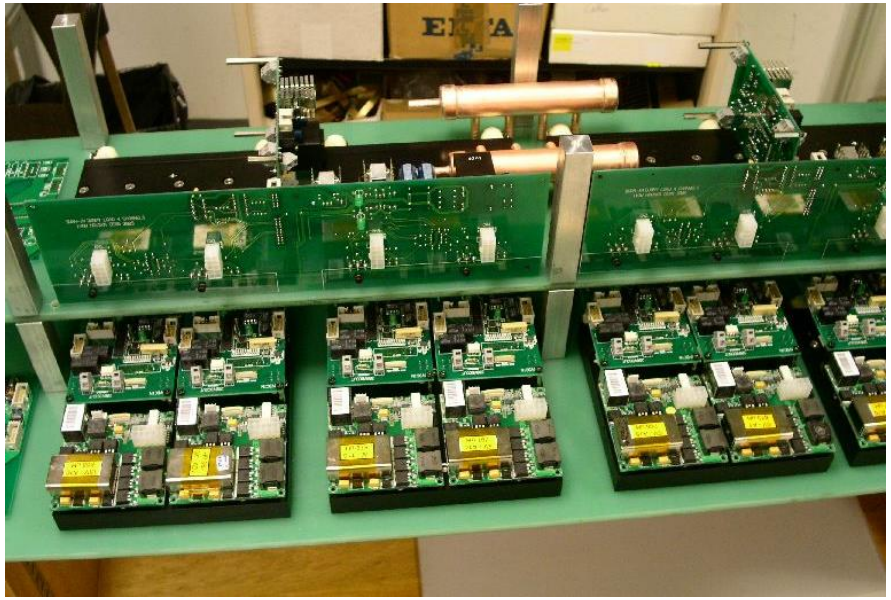
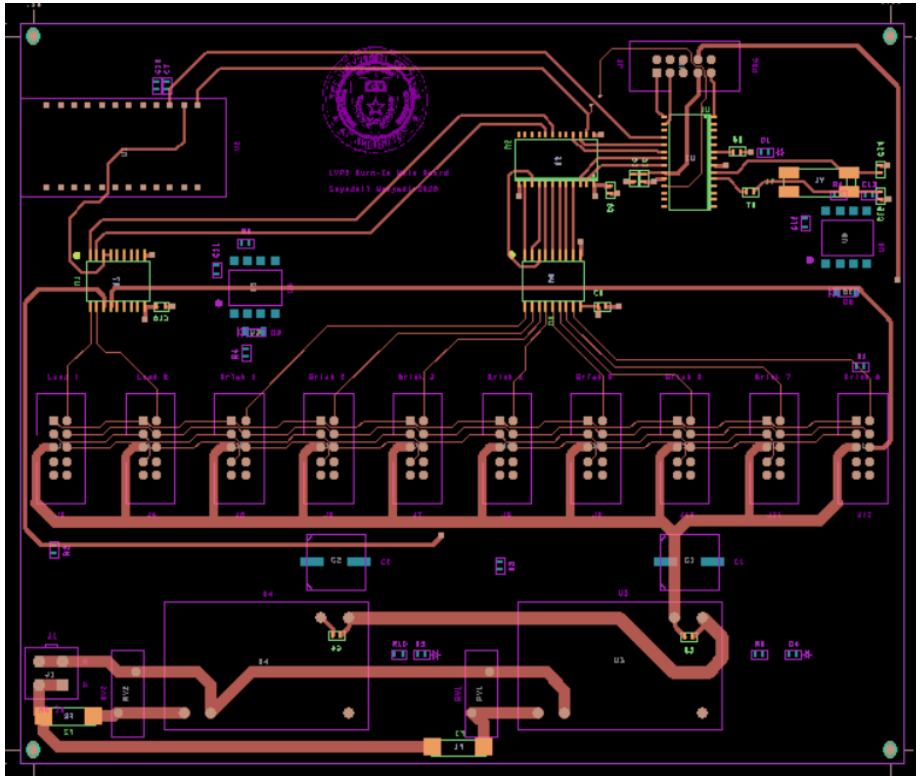
Legacy Burn-in test station

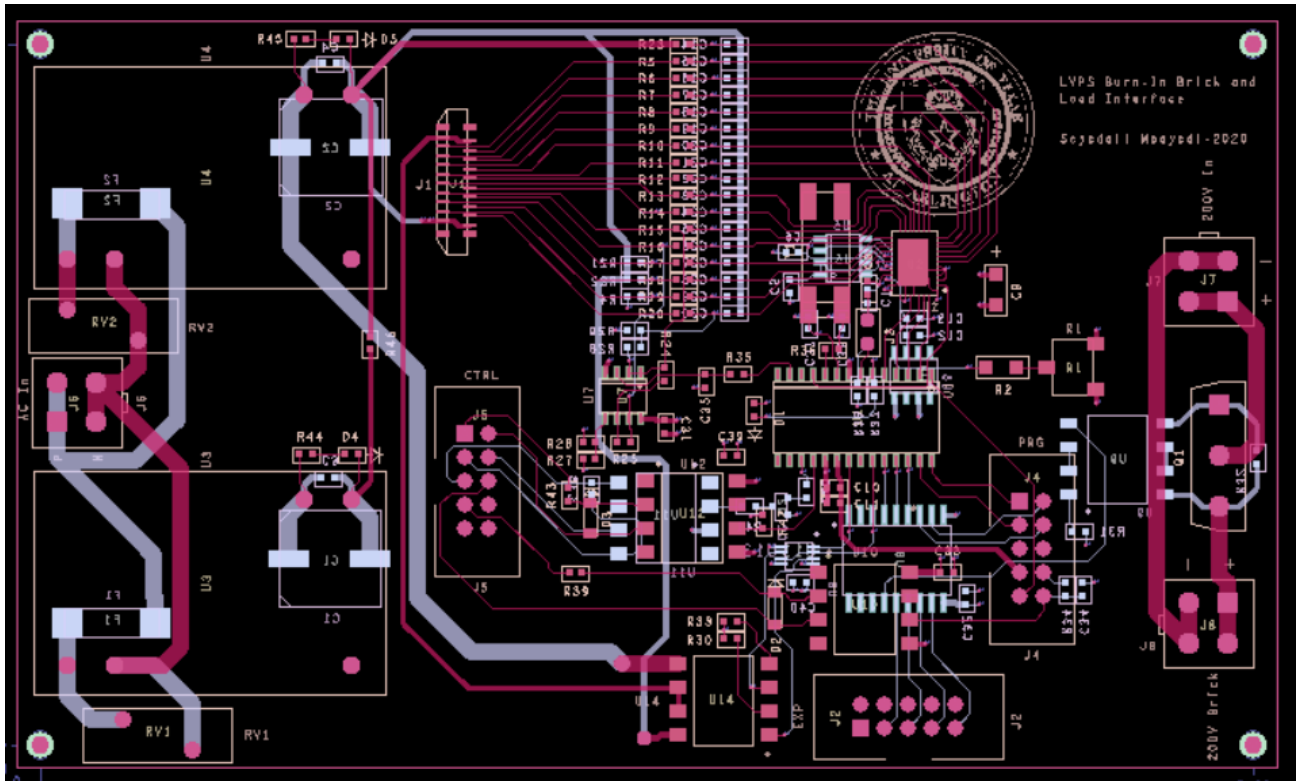


Main-board



- Function: A multiplexer to each readout board.

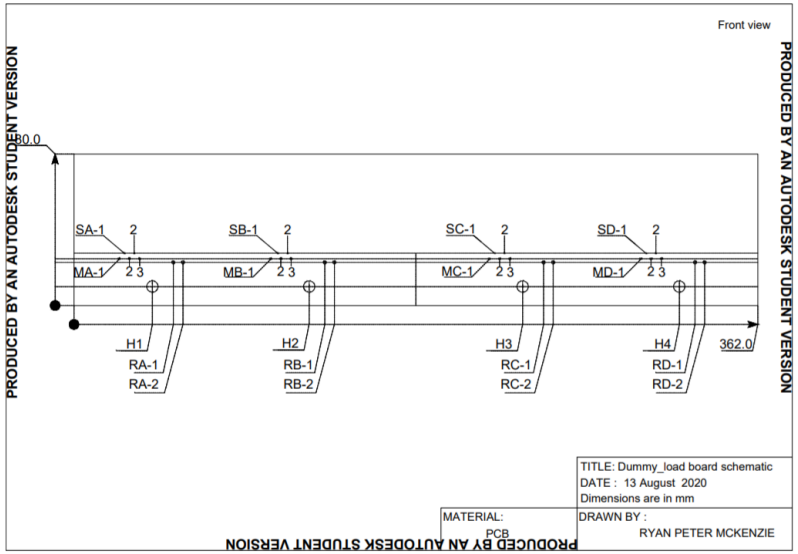
Interface-boards

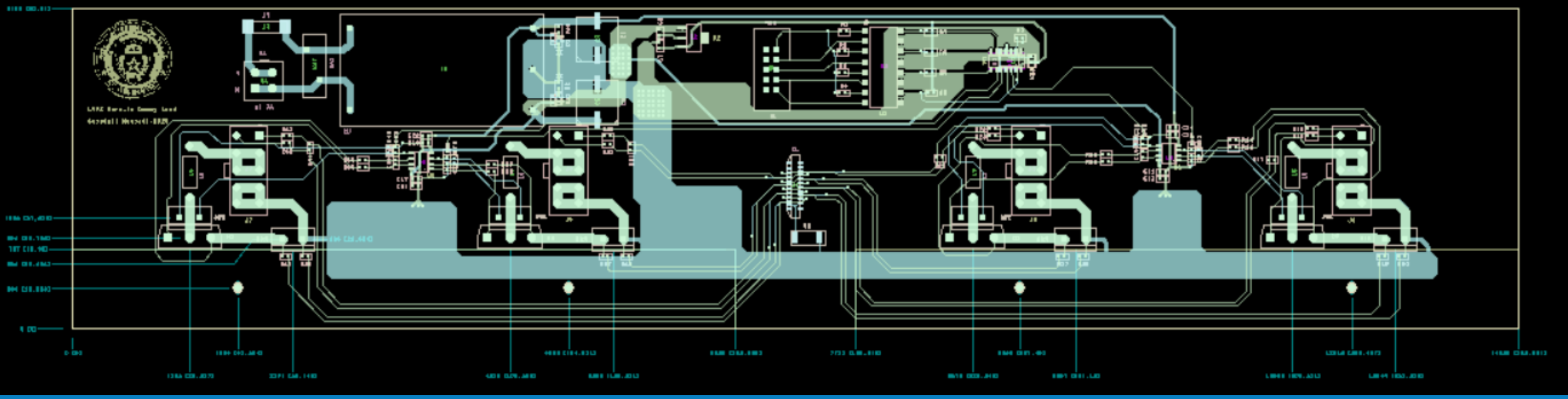


- Function: Interfacing between main board and Load/brick.
- Both the Brick Interface-board and Dummy-load interface board utilize the same PCB design.
- Variation occurs in the component populated on the board.

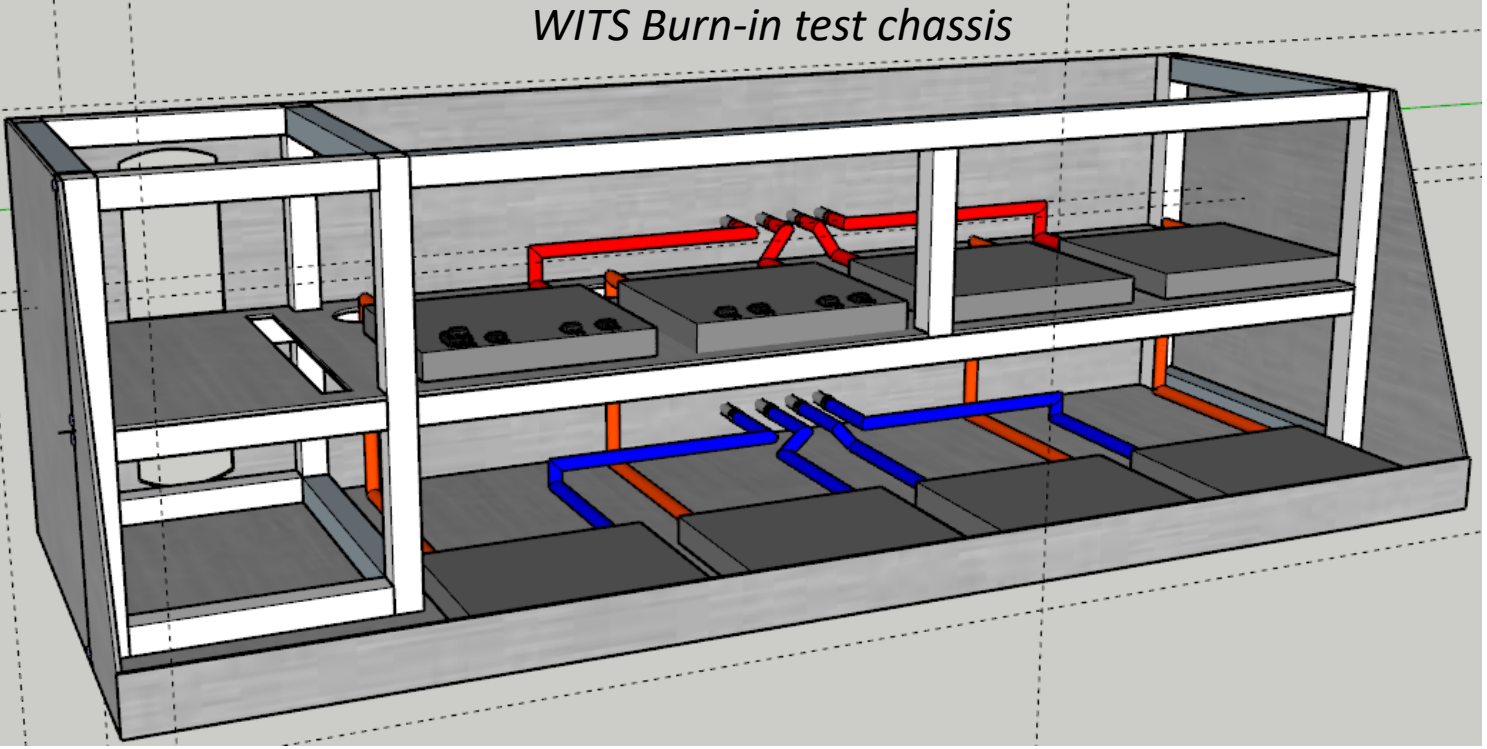
Dummy-Load board

- Function: Acts as a variable electronic load for the LVPS bricks.
- Converts power received into heat via MOSFETS.
- Heat dissipated via cooling plates.
- Both mechanical and electrical design need to considered in the PCB development.

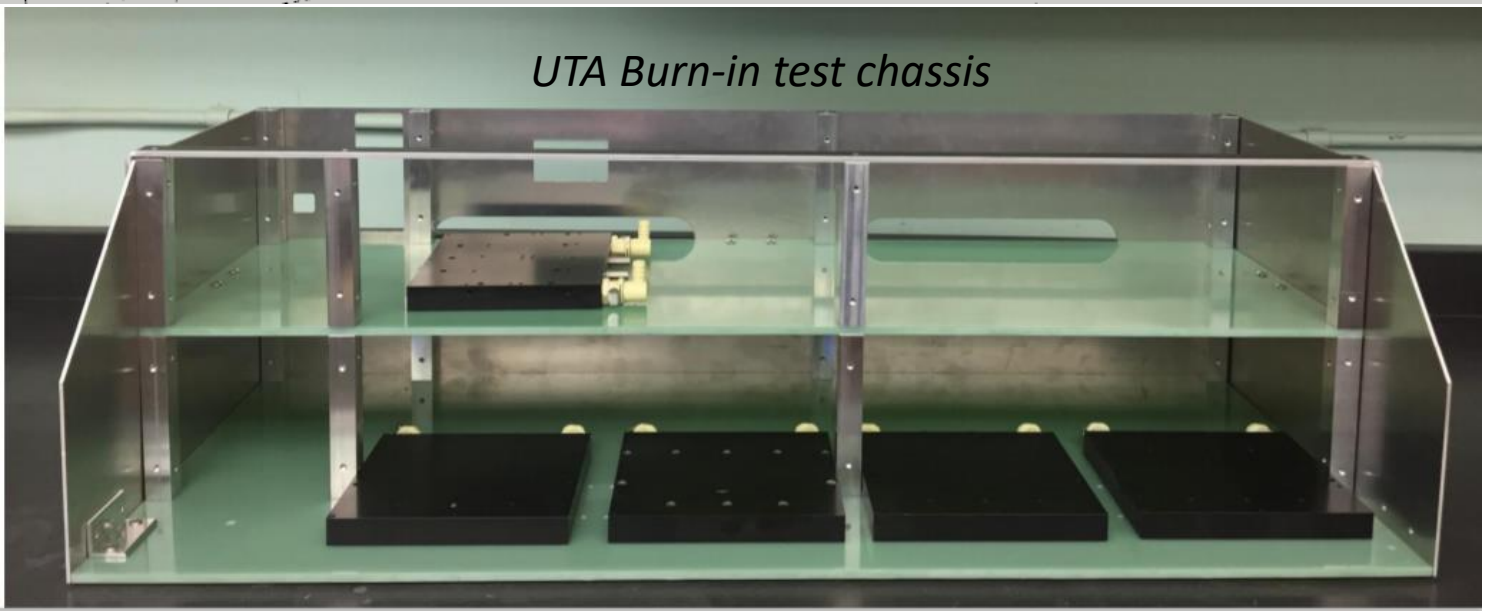




WITS Burn-in test chassis



UTA Burn-in test chassis



Burn-in chassis

- Function: To contain the testing apparatus as well as the LVPS bricks during testing.
- Key Considerations:

I. Safety – Grounding of 200VDC can be potentially fatal. The presence of coolant heightens the risk.

II. Due point – Condensation within the chassis is inherently undesirable.

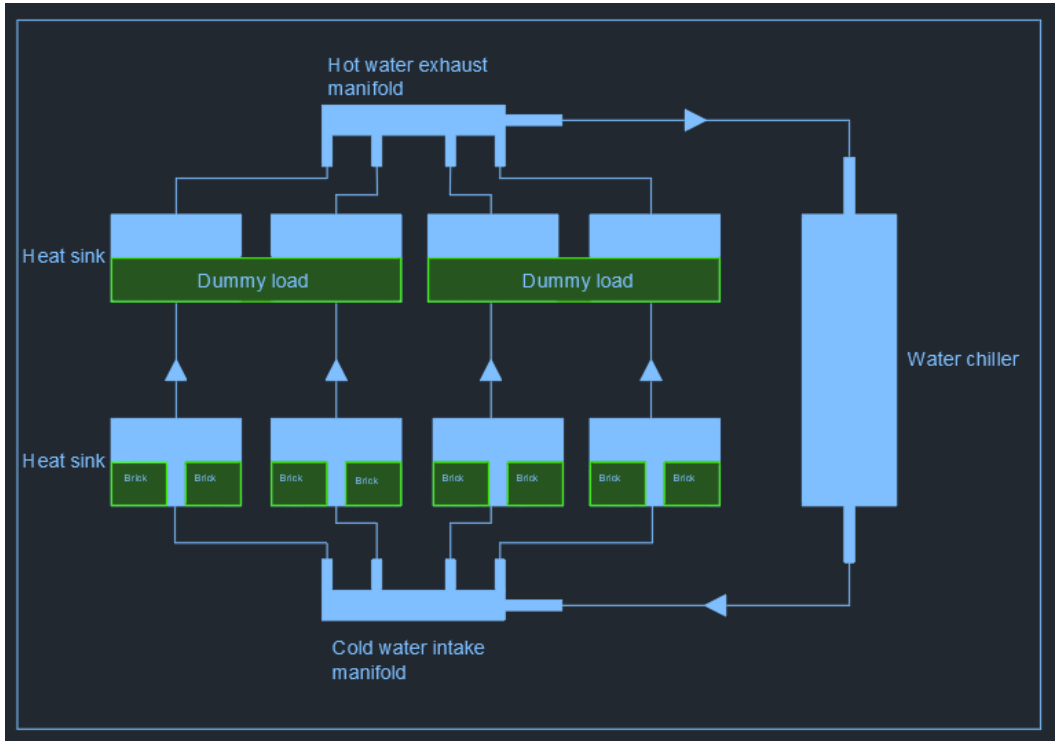
III. Accommodate PCB's and cooling plates.

Burn-in station cooling block diagram

- Function: To extract heat from the dummy-loads and LVPS bricks.
- Considerations:

I. Total heat to be extracted ~ 750 W
II. Ensuring bricks receive 15°C coolant.
III. Require 86L/h per branch,
IV. Ensuring consistent flow rate.

- Additional flow meter to be added.

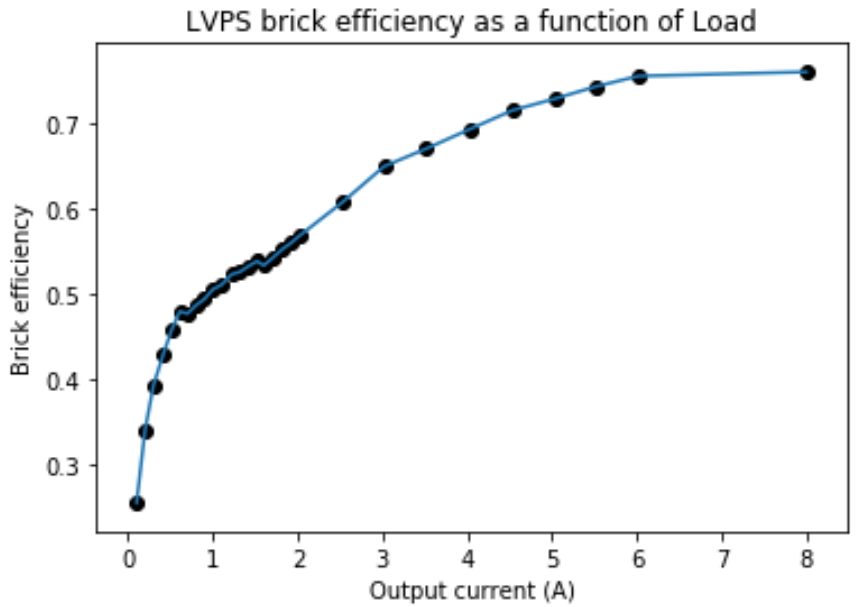


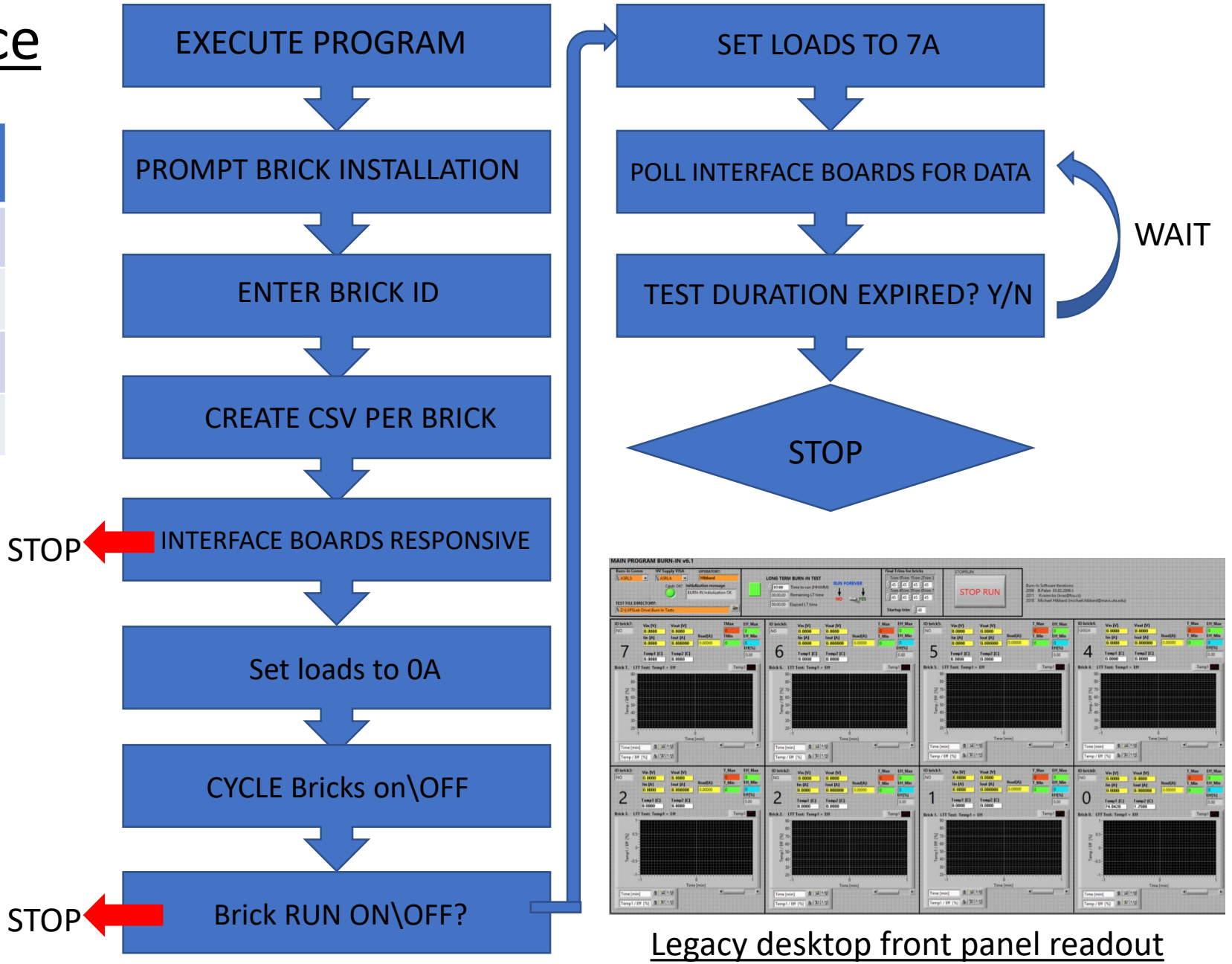
Water chiller

Water manifold

A Burn-in test sequence

Parameter	Value
Time duration	6 hours
Temperature	80°C
Brick Load	7A
Startup cycles	30+





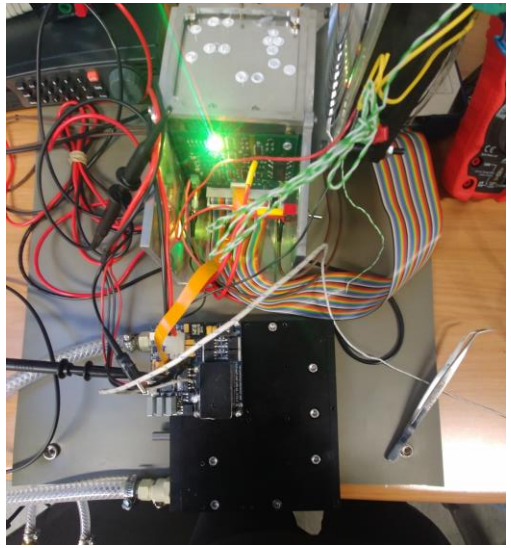
Legacy desktop front panel readout

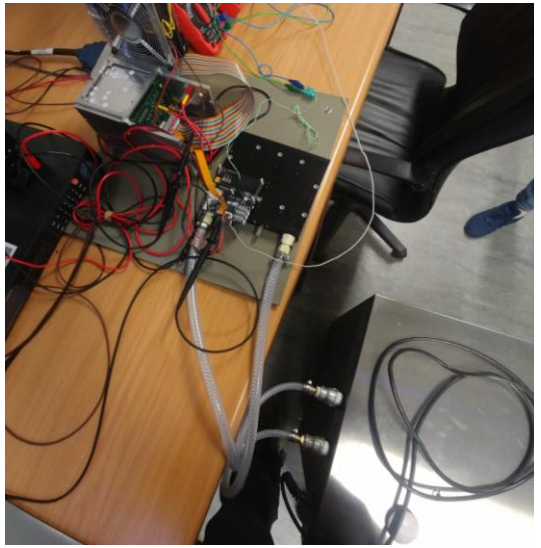
Burn-in station summary

- LVPS design and testing is an important step in the ATLAS TileCal Upgrade.
- Burn-in testing facility was designed:
  - Test chassis
  - Cooling system
  - Water chillers
  - Custom PCB's
  - Control software

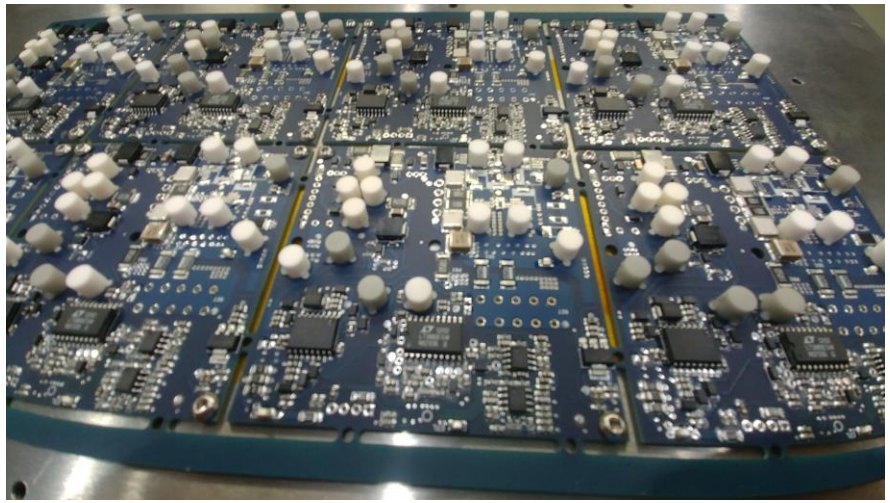
- Preliminary testing of Latest version of Hybrid LVPS bricks currently ongoing.

Thermal testing of new LVPS bricks while awaiting Burn-in components.

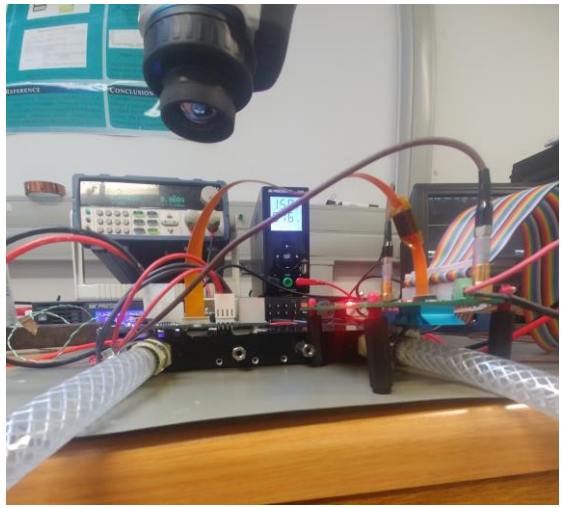


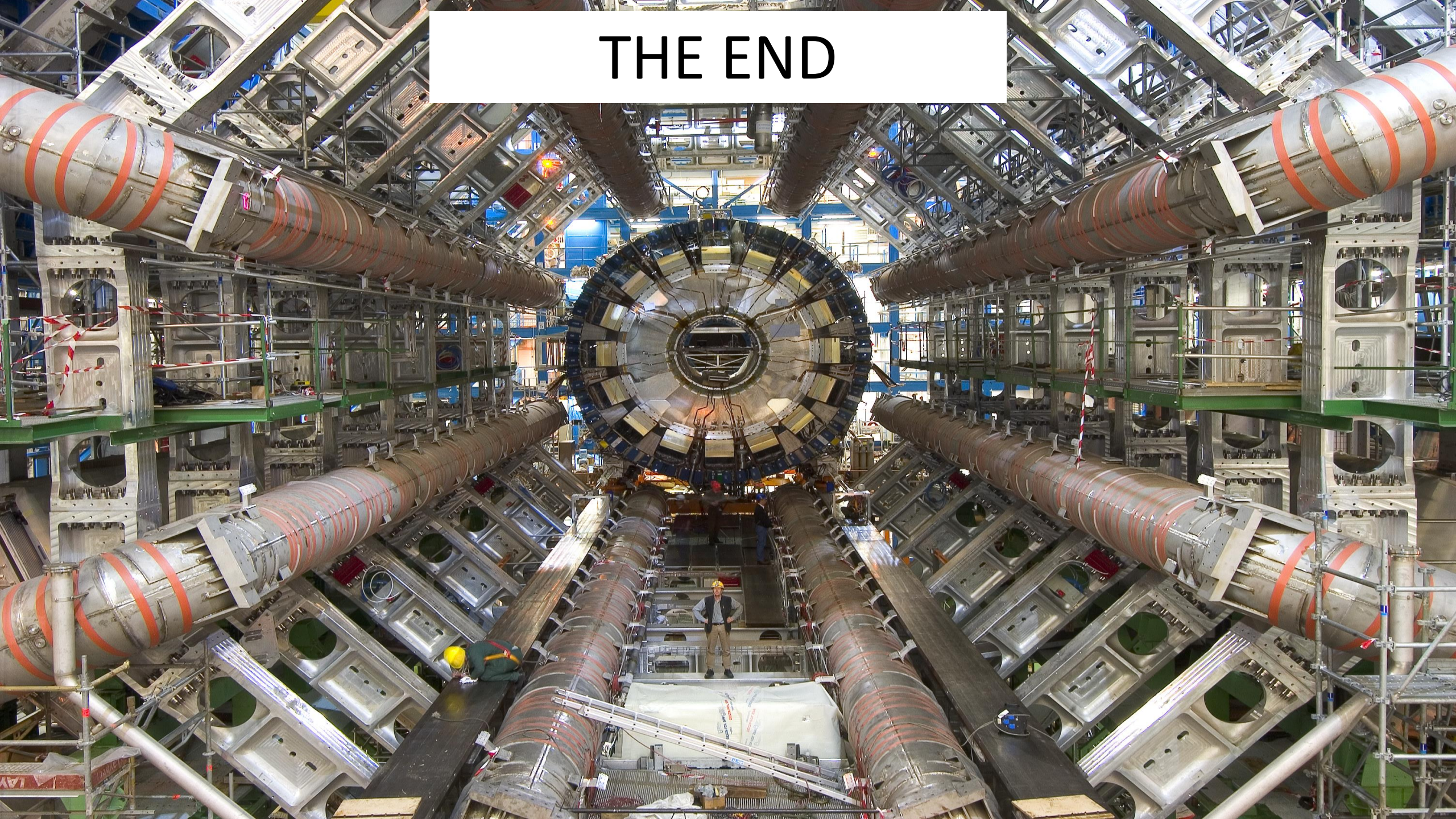


Latest Hybrid V8.4.2 Brick produced in SA.



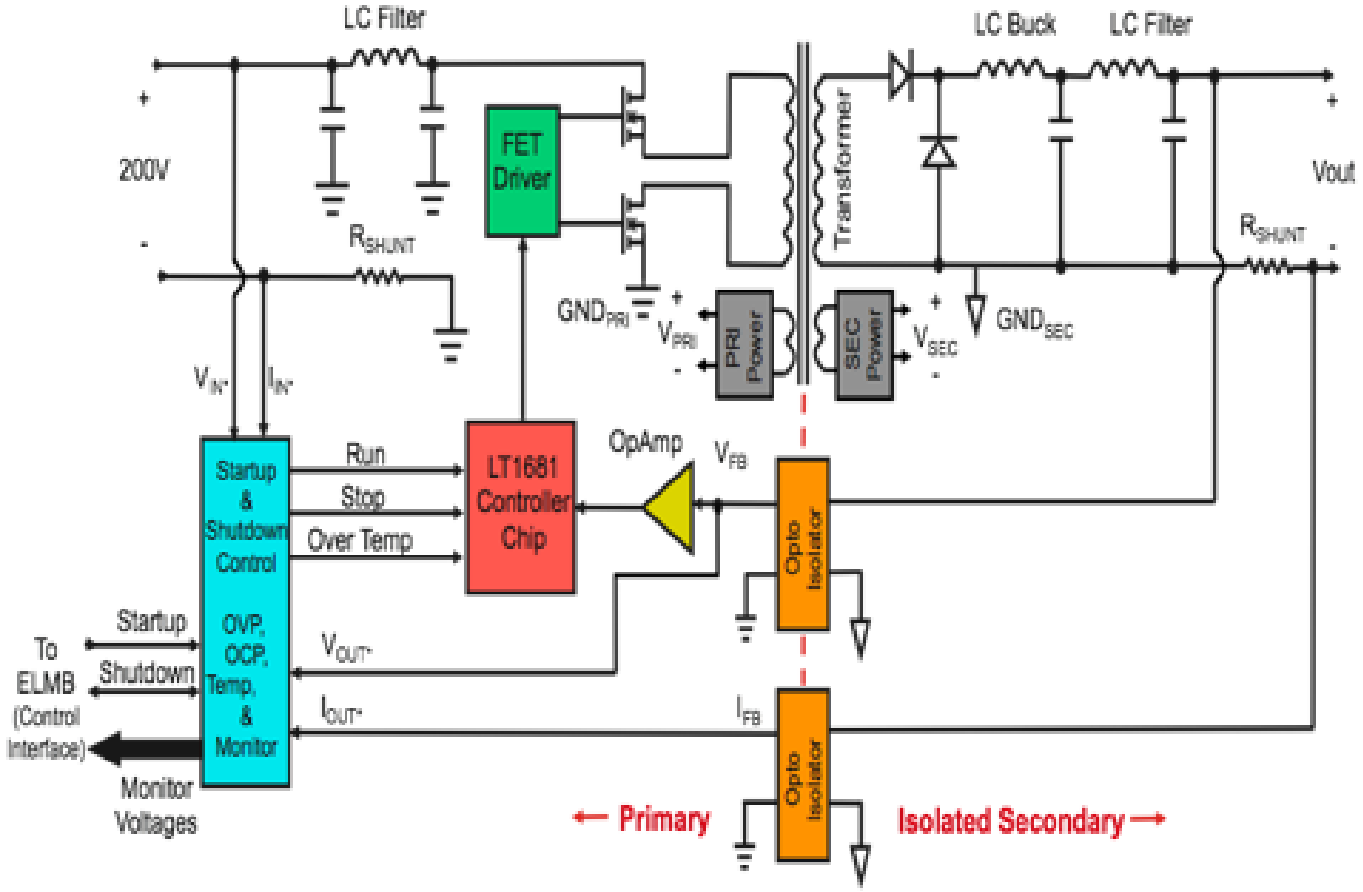
Thermal imaging camera




THE END

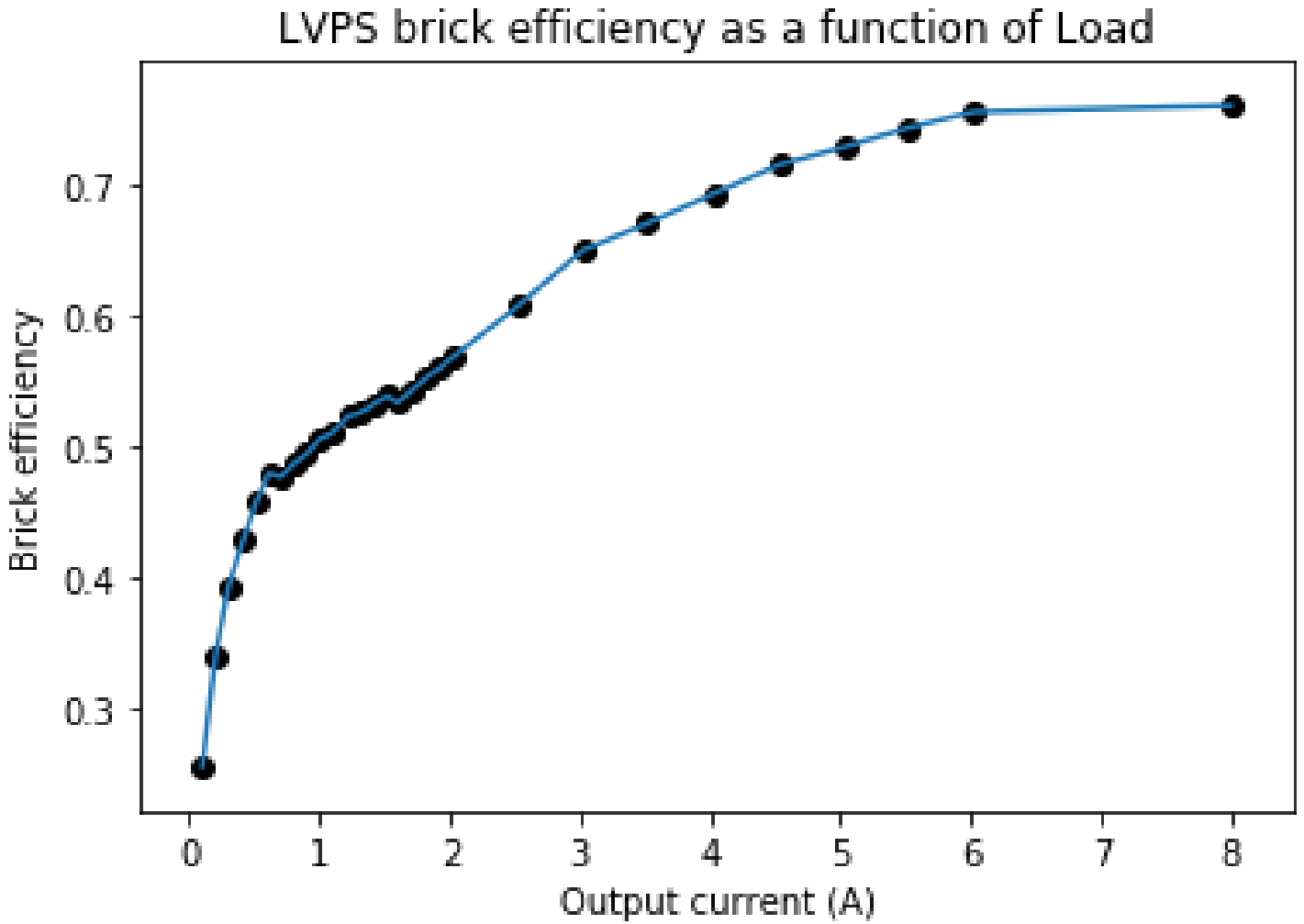
Backup slides

LVPS Brick

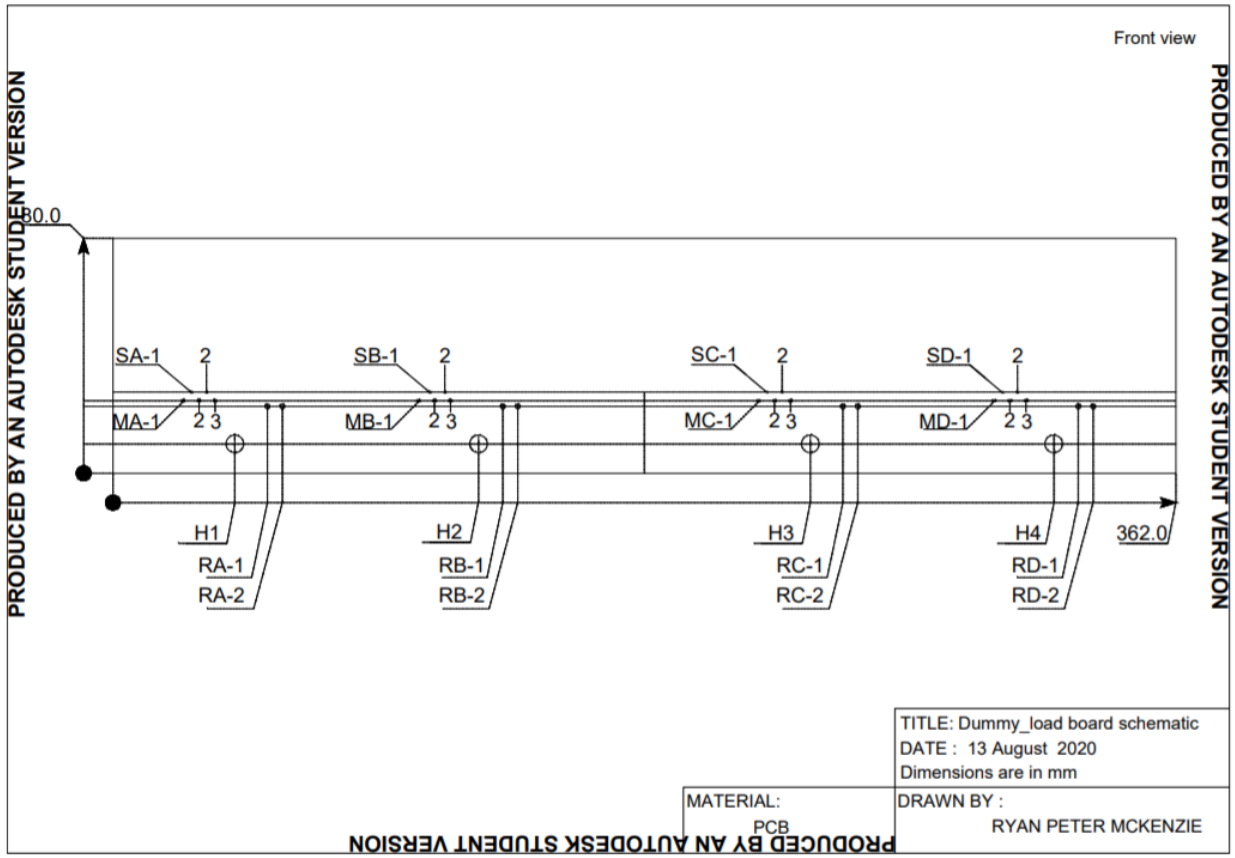


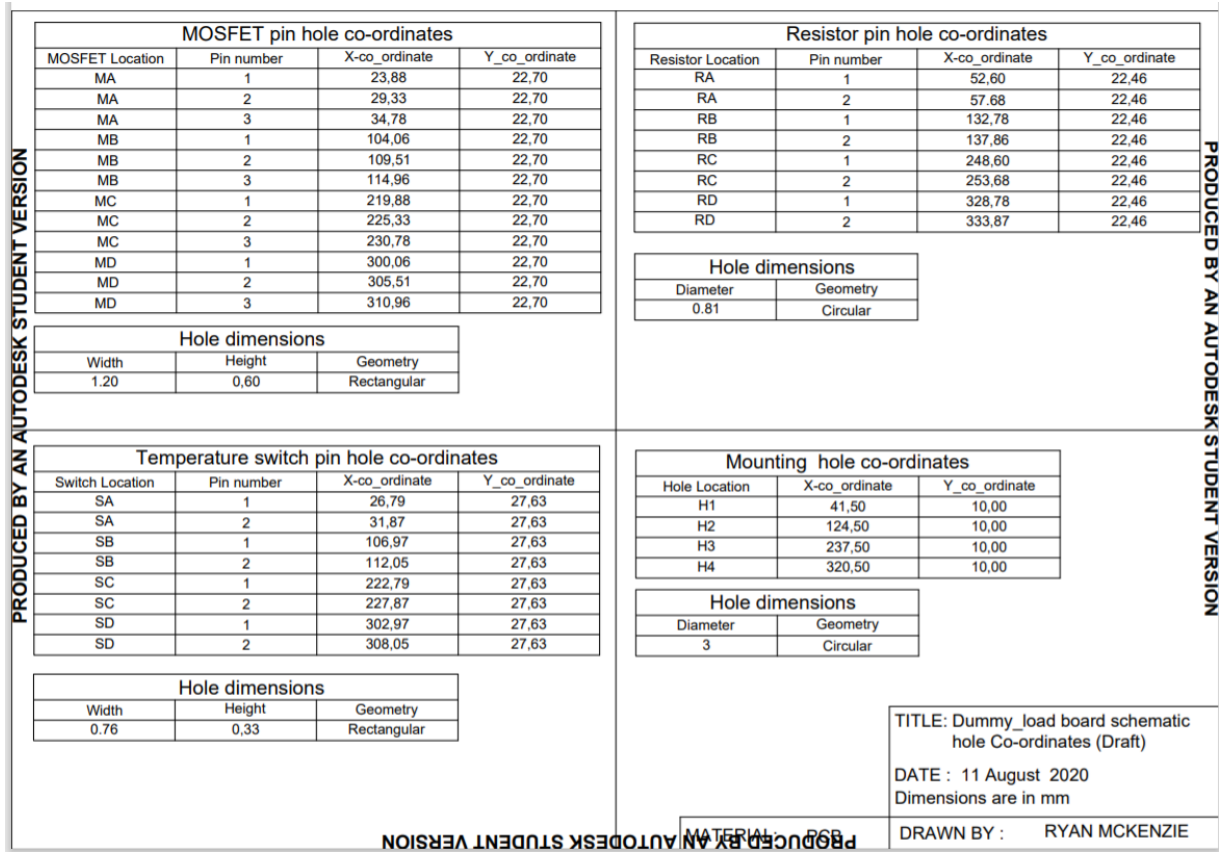
- LT1681 Controller Chip: Heart of design
- FET Drivers: Drive the Field Effect Transistors.
- FET's: When conducting current flows to the primary windings of the transformer which transfers energy to the secondary windings.
- Opto-Isolators: Provide voltage feedback for controlling the output voltage.
- Shunt Resistor: For measuring the output current
- Protection circuitry: Over Current Protection , Over Voltage Protection,

LVPS Efficiency



Dummy-load board mechanical design





MOSFET pin hole co-ordinates

MOSFET Location	Pin number	X-co_ordinate	Y_co_ordinate
MA	1	23,88	22,70
MA	2	29,33	22,70
MA	3	34,78	22,70
MB	1	104,06	22,70
MB	2	109,51	22,70
MB	3	114,96	22,70
MC	1	219,88	22,70
MC	2	225,33	22,70
MC	3	230,78	22,70
MD	1	300,06	22,70
MD	2	305,51	22,70
MD	3	310,96	22,70

Hole dimensions

Width	Height	Geometry
1.20	0,60	Rectangular

Resistor pin hole co-ordinates

Resistor Location	Pin number	X-co_ordinate	Y_co_ordinate
RA	1	52,60	22,46
RA	2	57.68	22,46
RB	1	132,78	22,46
RB	2	137,86	22,46
RC	1	248,60	22,46
RC	2	253,68	22,46
RD	1	328,78	22,46
RD	2	333,87	22,46

Hole dimensions

Diameter	Geometry
0.81	Circular

Temperature switch pin hole co-ordinates

Switch Location	Pin number	X-co_ordinate	Y_co_ordinate
SA	1	26,79	27,63
SA	2	31,87	27,63
SB	1	106,97	27,63
SB	2	112,05	27,63
SC	1	222,79	27,63
SC	2	227,87	27,63
SD	1	302,97	27,63
SD	2	308,05	27,63

Hole dimensions

Width	Height	Geometry
0.76	0,33	Rectangular

Mounting hole co-ordinates

Hole Location	X-co_ordinate	Y_co_ordinate
H1	41,50	10,00
H2	124,50	10,00
H3	237,50	10,00
H4	320,50	10,00

Hole dimensions

Diameter	Geometry
3	Circular

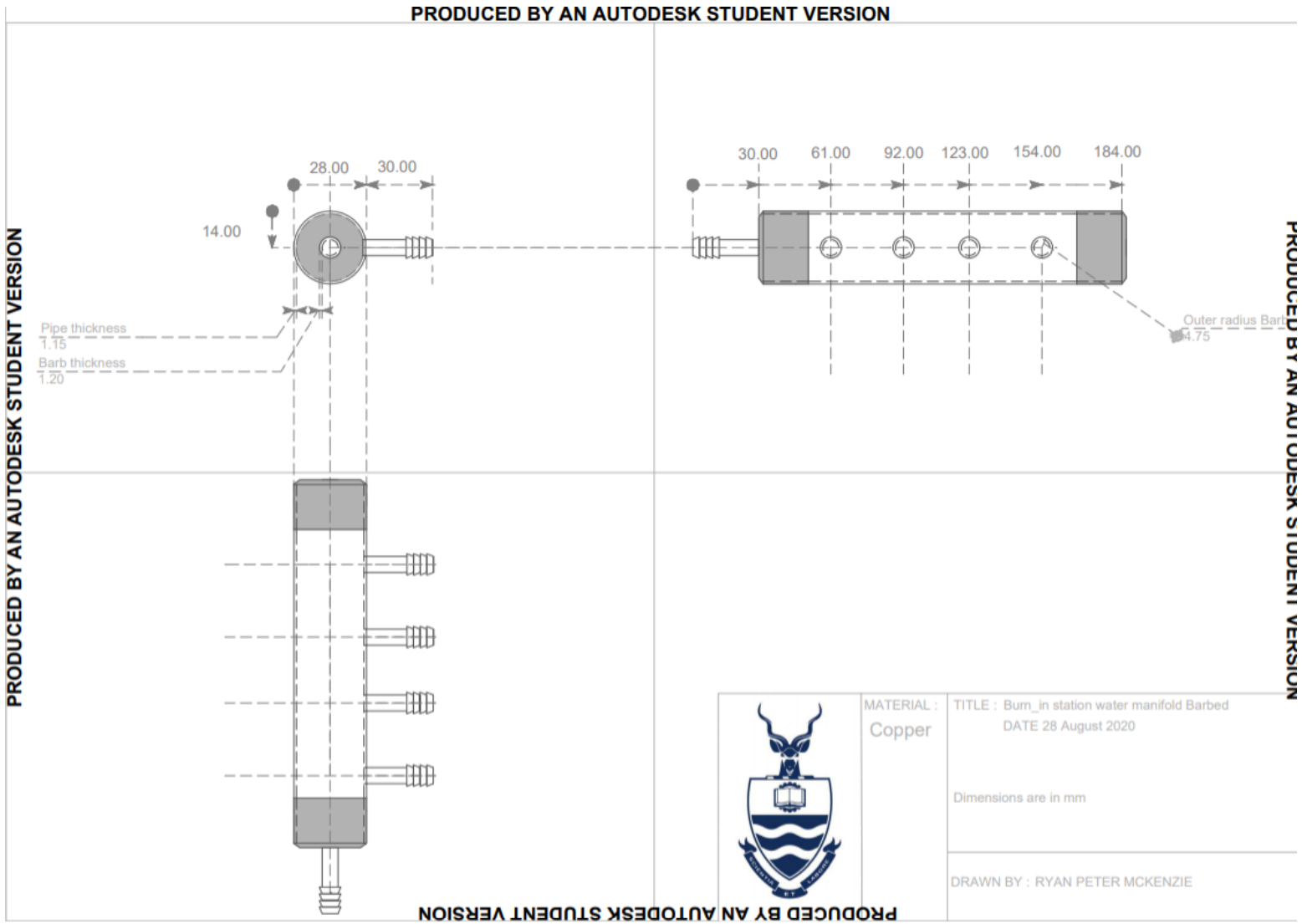
LVPS cooling plates

Inlet

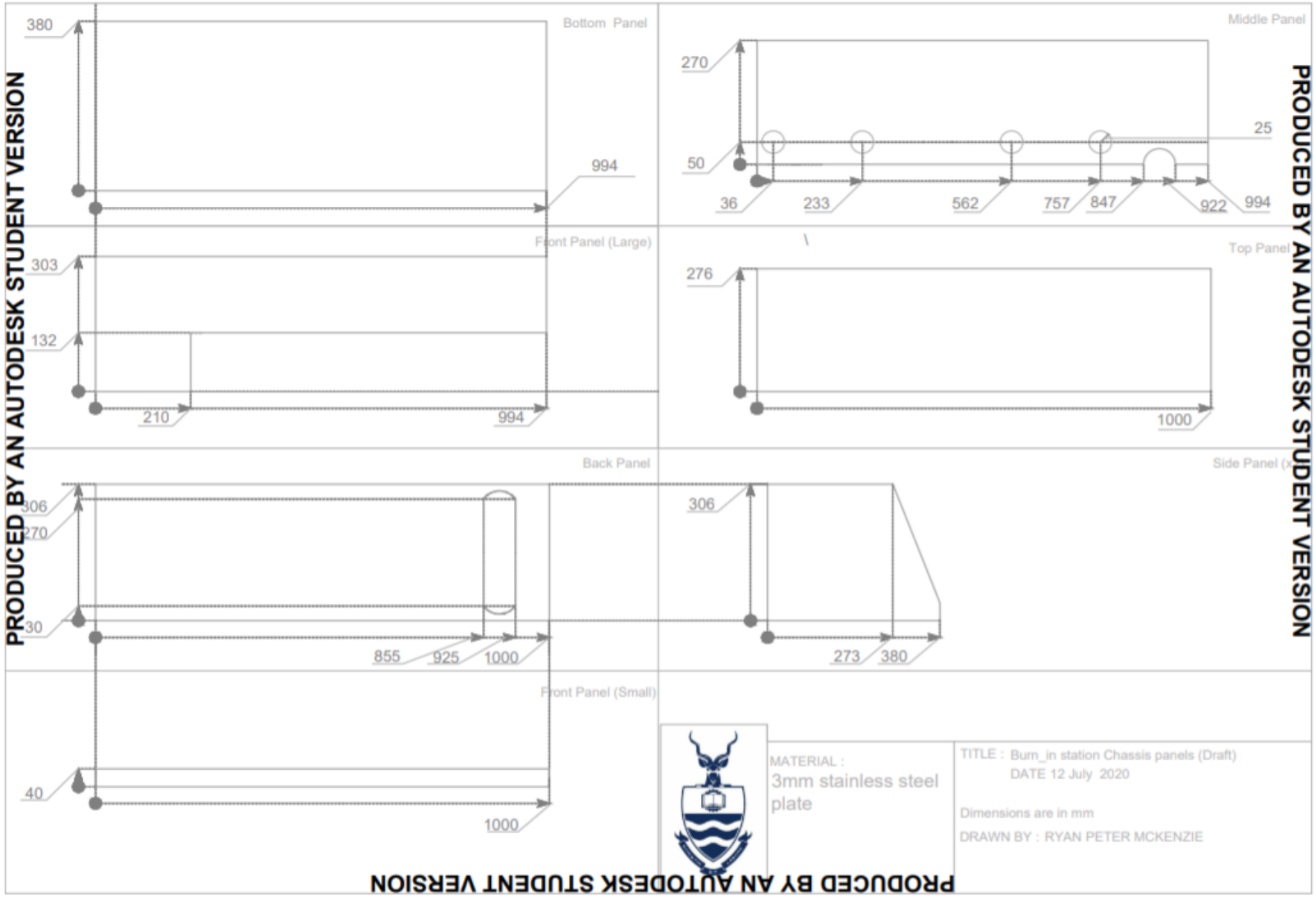
Outlet

Inner coolant channel

Water Manifold



Burn-in chassis panel schematics



Front-end electronics

Consists of:

- 12×PMTs,
- 12×FENICS and 12 active dividers → read out 6 TileCal cells,
- 1×MainBoard, 1×DaughterBoard,
- 1×HV passive board