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SLVS Transmitter and Receiver for CBM MUCH ASIC

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Scalable Low Voltage Signaling (SLVS) Transmitter (Tx) and Receiver (Rx) IP blocks are designed in the UMC 180 nm CMOS technology as component of the readout ASIC for the muon chambers (MUCH) of the Compressed Baryonic Matter (CBM) experiment at FAIR (Darmstadt, Germany). These blocks are a prototype of the physical layer of the e-link interface that is used for ASIC-GBTx connection. The experimental results at 320 Mbit/s are presented.

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