Substrate noise isolation technique for mixed-signal ASICs in particle physics instrumentation

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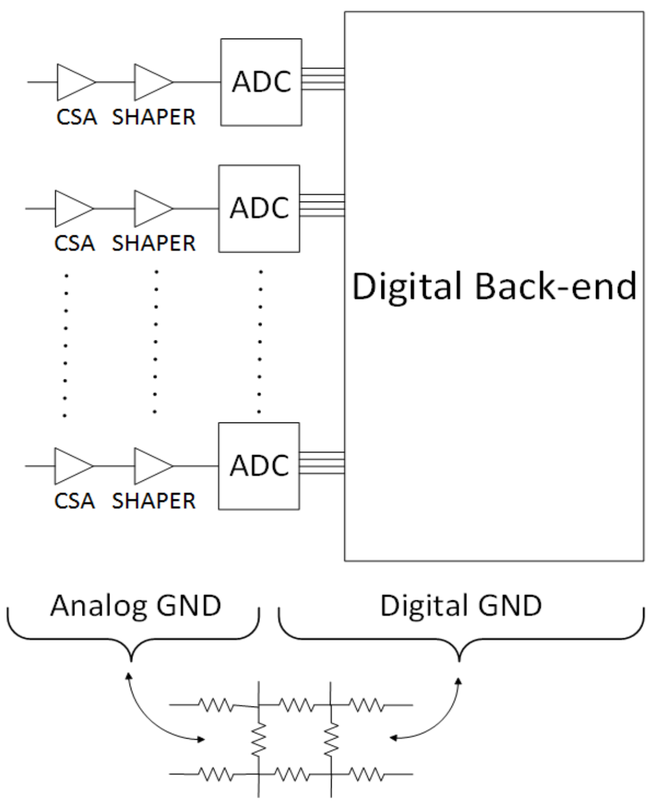
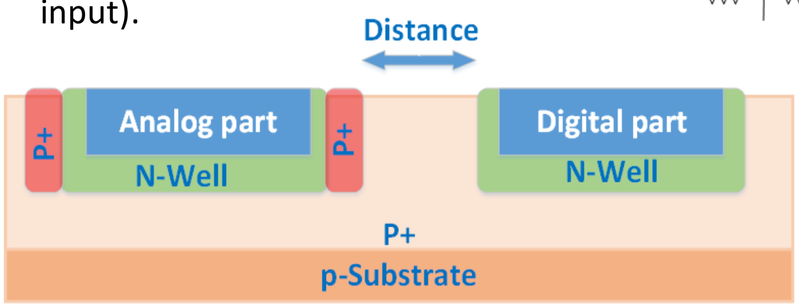
Abstract

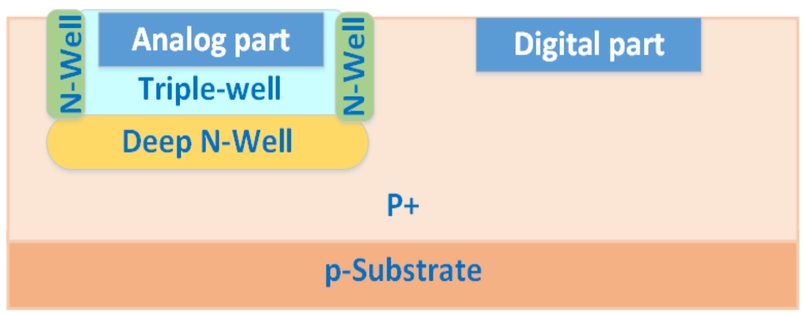
The paper describes methodology of substrate noise isolation for ASICs implemented in the CMOS processes. Up-to-date CMOS technologies allow embedding the digital data processing blocks into the same die as the readout analog part. This significantly improves the functionality and complexity of the readout ASICs. In fact performance of the precision analog circuits (e.g. charge sensitive amplifier, shaper, etc.) can suffer from the additional noise contribution from the high-frequency digital part. This work describes the ways of decrease the substrate noise influence on the sensitive circuits of the readout channels. Simulation results and comparison of different isolation approaches are considered in the paper.

Noise distribution over the substrate

Up-to-date front-end ASICs are complicated mixed-signal SoC. Besides the precision analog part the chips include ADC with sampling rate of tens of MSps and fast digital blocks operating at rates of hundreds of MHz. Although the ground nodes are separated in the metal layers, they in fact are connected via the chip substrate. The substrate has a non-zero resistance. Hence the noise distributes over the whole die and can affect precision and sensitive nodes (e.g. CSA input).





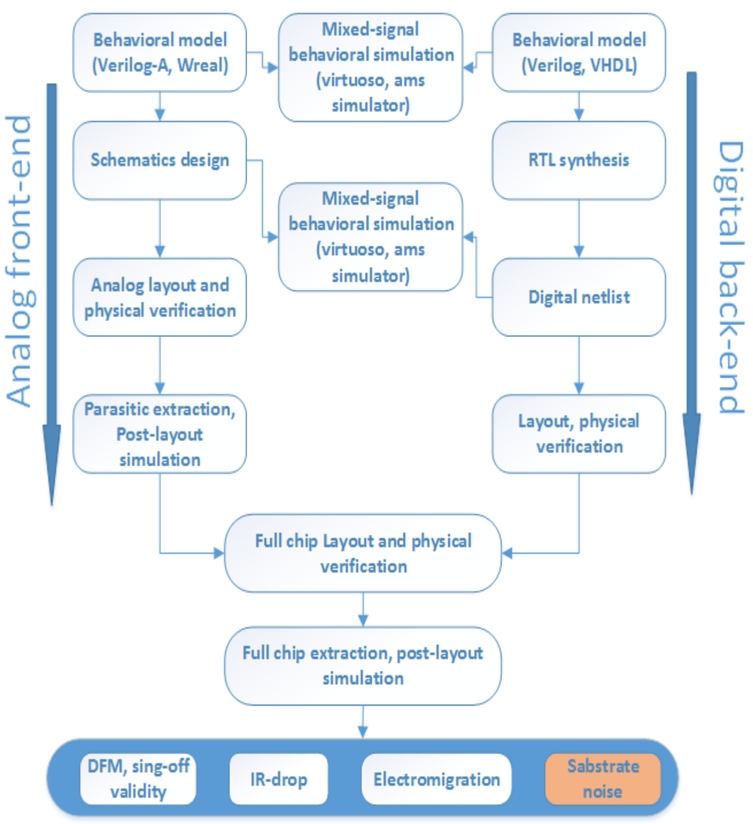


Isolation Technique:

- Differential structure
- N-well
- PP-Guard rings
- Triple-well processes
- Distance between noise source and "victim"
- Metal layers Shielding

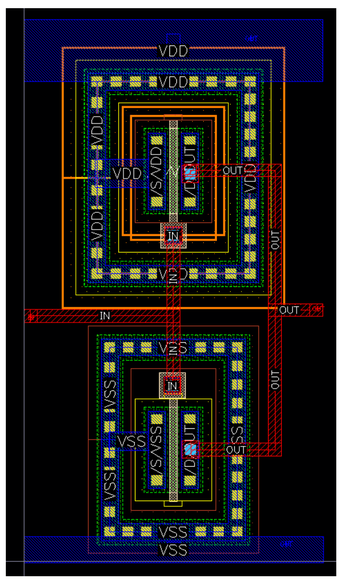
Design flow

State-of-art EDAs allow analyzing the noise distribution over the die for different CMOS processes. The noise depends on the substrate structure (e.g. type, depth, doping profiles etc.). Having the substrate parameters, one can synthesize the substrate macro model. The substrate macro model includes the information about the distributed resistance and capacitance. By this model it is possible to extract the stray elements into the schematics and simulate the effects of the substrate noise. This makes possible to analyze the noise distribution and its influence on the sensitive elements of the analog readout.

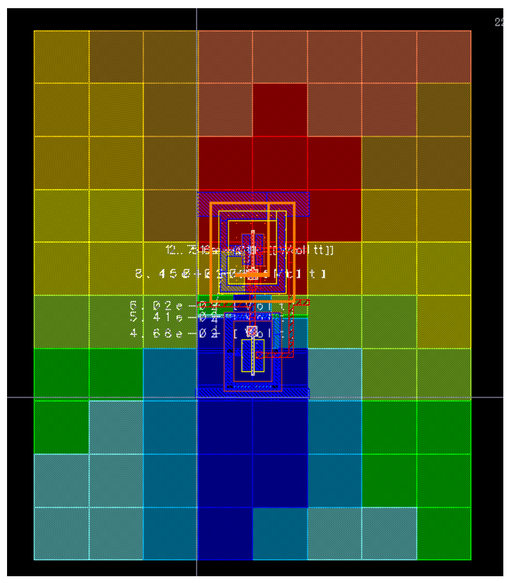


Simulation results

Simulation results for 0.18 um CMOS process is provided by Cadence QRC and SND design flow. The substrate noise distribution was simulated for CMOS inverter layout. A noise source point is the output of inverter. Voltage amplitude swing – 1.8 V at 1 GHz.



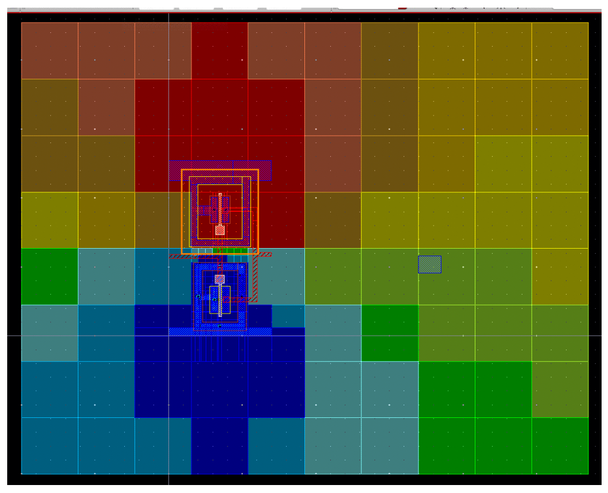
test layout



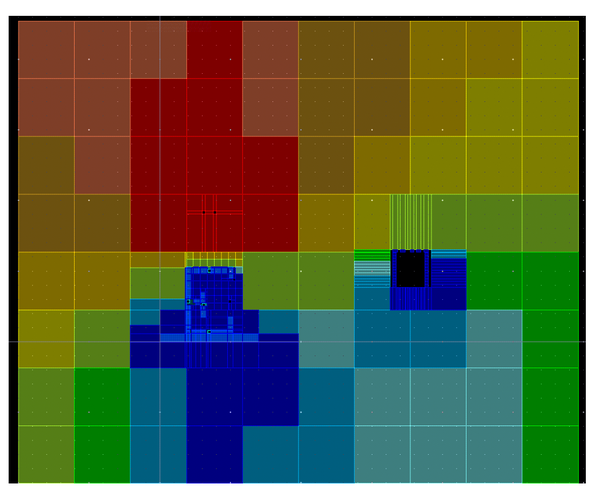
Substrate noise distribution

Color map. S_{21} value in dB

The influence of the noisy inverter output on the noise acceptor (metal fragment on the right side of the diagram below) has been studied for the case of non-isolated element and metal piece with a P+ guard ring.



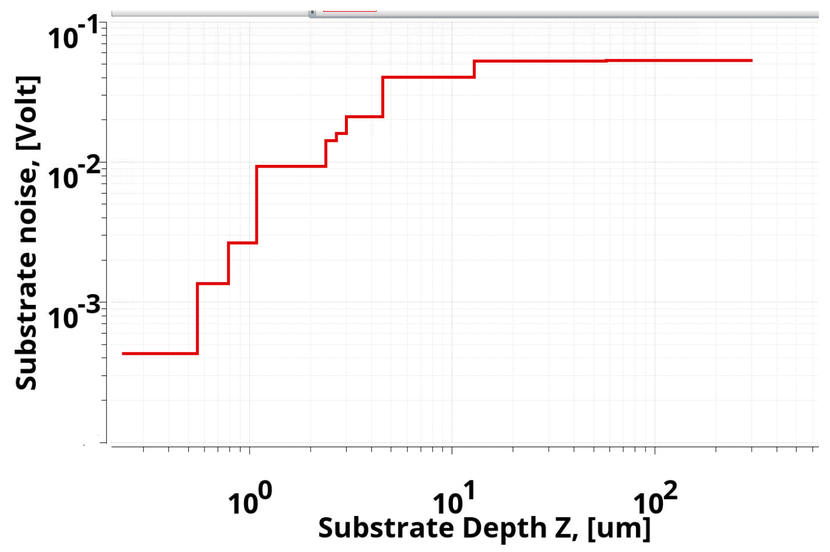
Non-isolated metal. S21: – 25 dB



Metal in PP-Guard ring. S21: – 40 dB

Dependences of the noise distribution on the substrate depth and distance between the noise aggressor and victim have been obtained as well.

Distance	S21
1u	- 0.5 dB
10 um	- 21.3 dB
20 um	- 22.4 dB
30 um	- 22.4 dB
50 um	- 22.4 dB
100 um	- 22.5 dB



Conclusions

The substrate noise analysis design flow and methods of sensitive elements isolation have been presented. The paper describes simulation results of the substrate noise in 180 nm CMOS process. The noise distribution over the surface on depth as well as the dependence of the noise amplitude on the distance to the source are shown.

Acknowledgements

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