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Substrate noise isolation technique for mixed-signal ASICs in particle physics instrumentation

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The paper describes methodology of substrate noise isolation for ASICs implemented in the CMOS processes. Up-to-date CMOS technologies allow embedding the digital processing blocks into the same die as the readout analog part. This significantly improves the functionality and complexity of the readout ASICs. In fact performance of the precision analog circuits (e.g. charge sensitive amplifier, shaper, etc.) can suffer from the additional noise contribution from the high-frequency digital part. This work describes the ways of decrease the substrate noise influence on the sensitive circuits of the readout channels. Simulation results and comparison of different isolation approaches are considered in the paper.

Primary author(s) : Mr. EVGENY, Malankin (NRNU MEPHI)

Presenter(s) : Mr. EVGENY, Malankin (NRNU MEPHI)

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