

Complex function block of processing and transferring asynchronous data for the IC of reading out the signals of multichannel detectors

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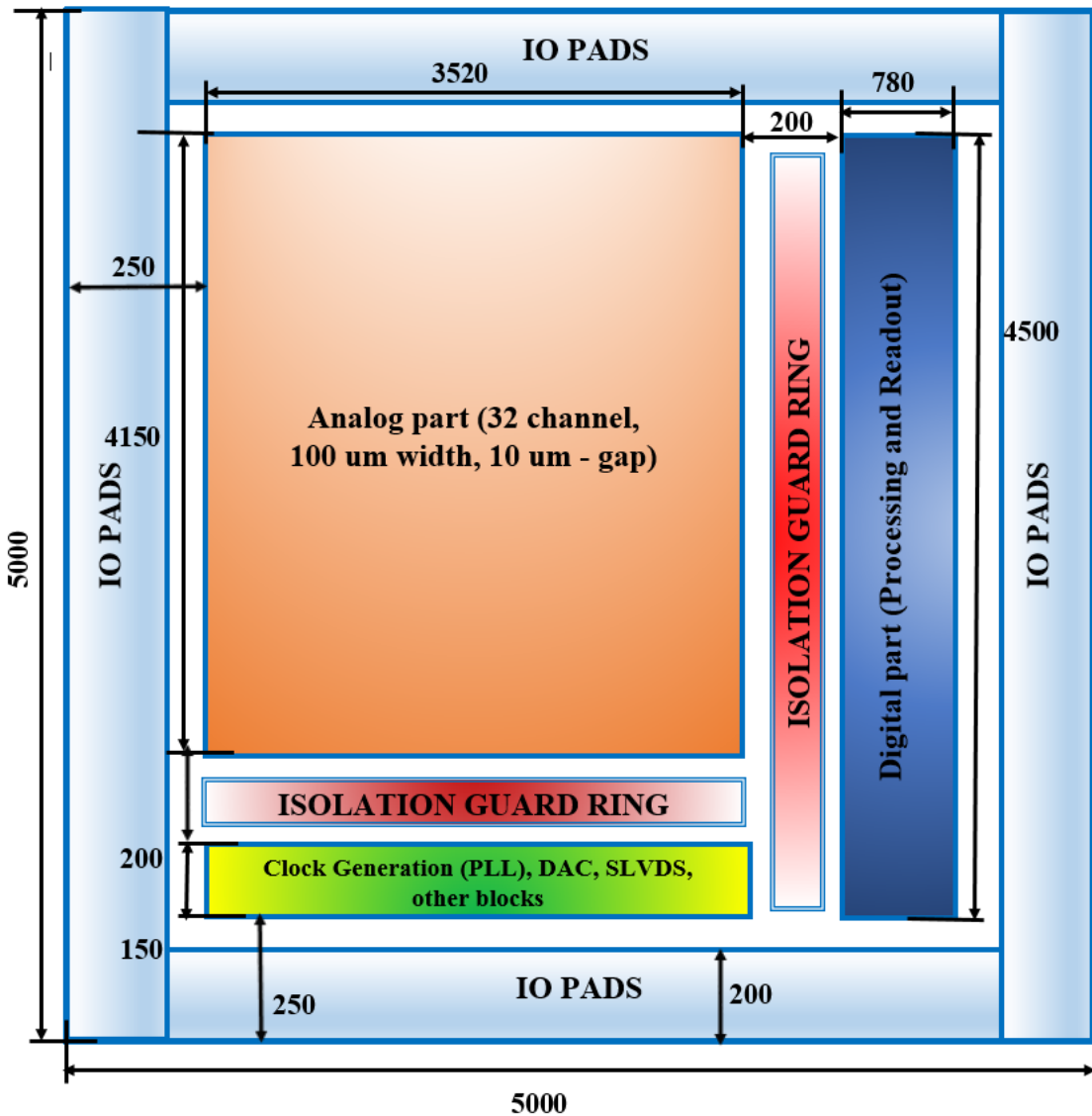
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Outline

- Floor plan
- CFP features
- CFP structure
- Data flow rate estimation
- Timestamp
- Peak detector
- GBT interface
- Present status

Floor plan



ASIC area

$$5000 \times 5000 \text{ } \mu\text{m} = 25 \text{ } mm^2$$

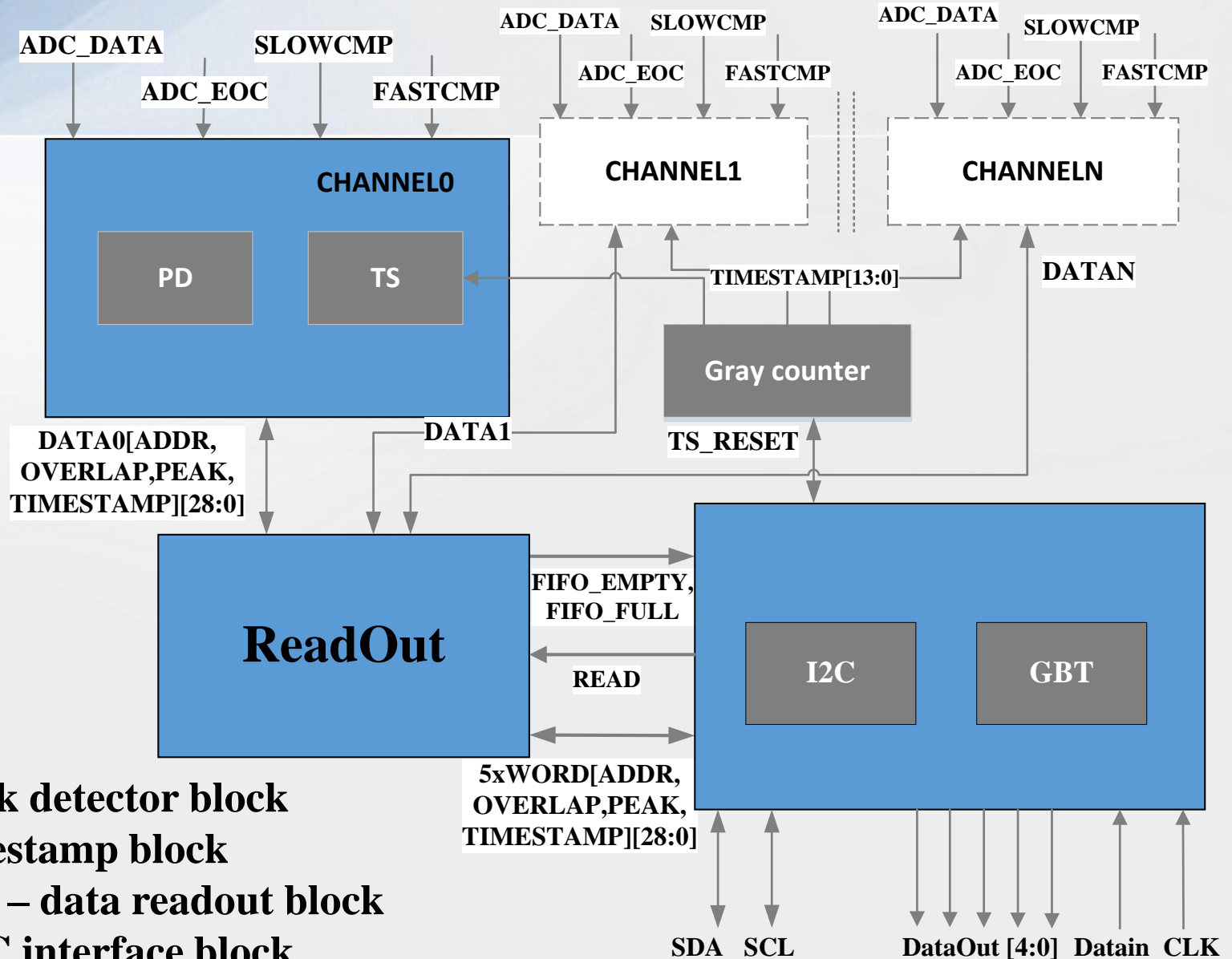
CFP (Digital part) ~ 14 % of the whole area

Technology - UMC 180 nm

CFP features

- 1. Timestamp generation**
- 2. Peak detection**
- 3. Data readout**
- 4. Data exchange with host via I2C/GBT interfaces**
 - 4.1 Global time synchronization**
 - 4.2 Slow control**
 - 4.2.1 Selective block resetting**
 - 4.2.2 Standby mode control**
 - 4.2.3 DACs codes setting**
 - 4.2.4 PD control**
 - 4.2.5 TS control**
 - 4.2.6 Readout fifos status monitoring**
 - 4.3 Payload data transfer to host**
- 5. ADC control**

CFP structure



PD – peak detector block

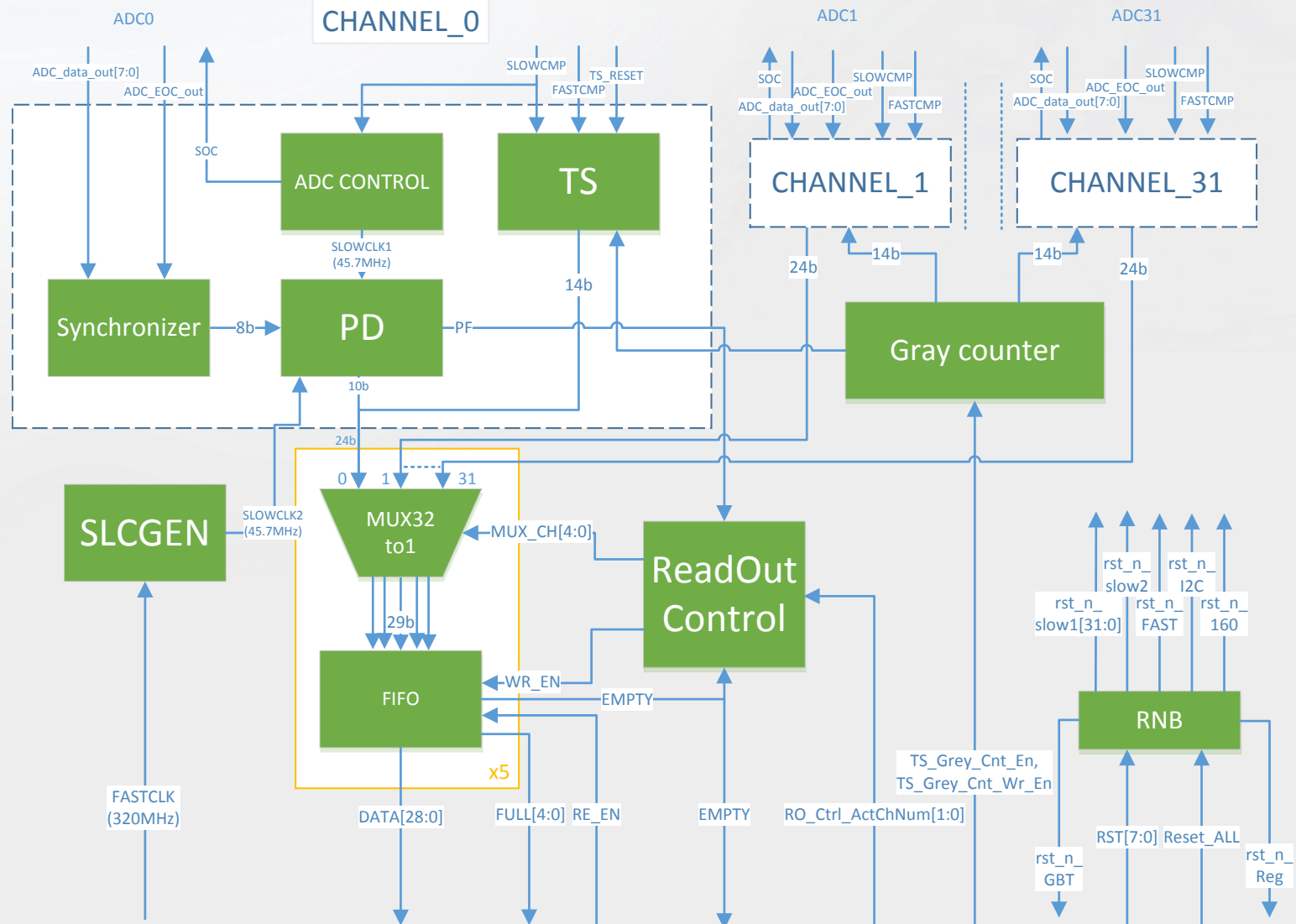
TS – timestamp block

ReadOut – data readout block

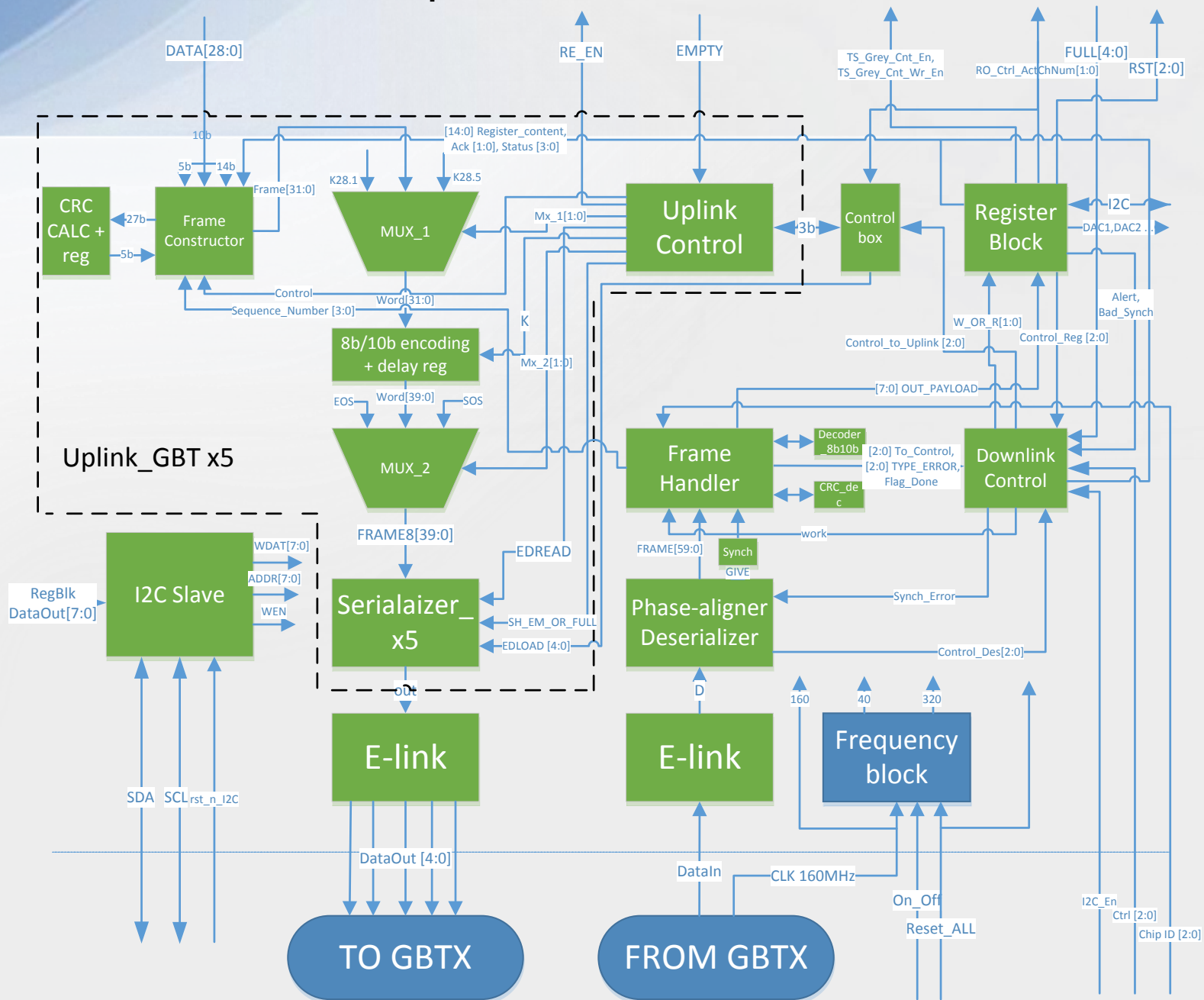
I2C – I2C interface block

GBT – GBTX interface block

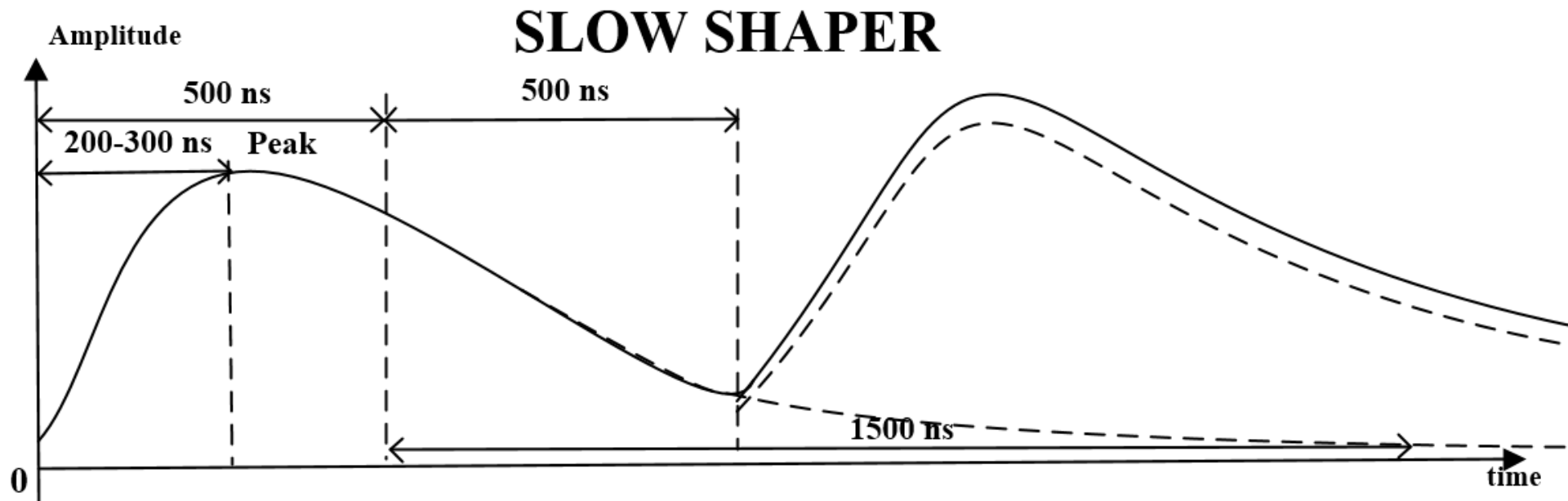
Structure of the data processing and readout channel



Interface part structure (GBT + I2C)



Data flow rate estimation



GBT interface:

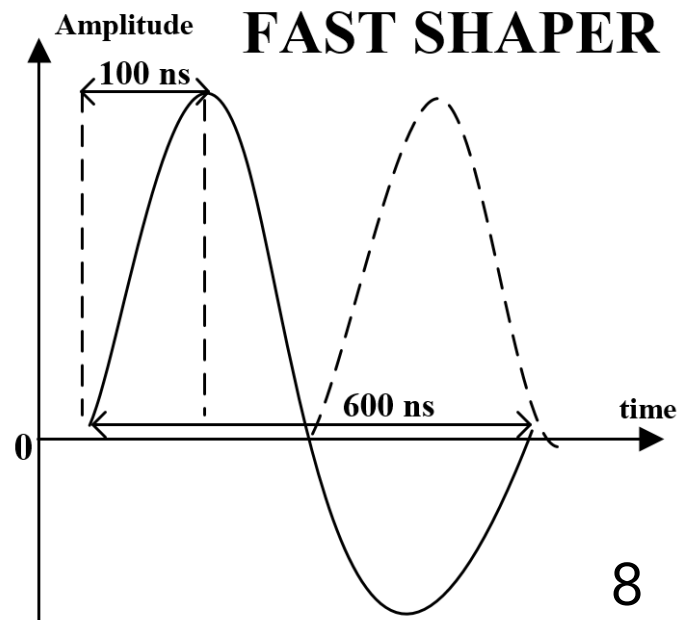
$5 \text{ бит} / 3.125 \text{ нс} = 1.6 \text{ Gb/s}$ (@ 320 MHz)

Data to send at 20% loading level:

$32 \text{ ch.} \times 0.2 \times 40 \text{ bit} \sim 256 \text{ bits}$

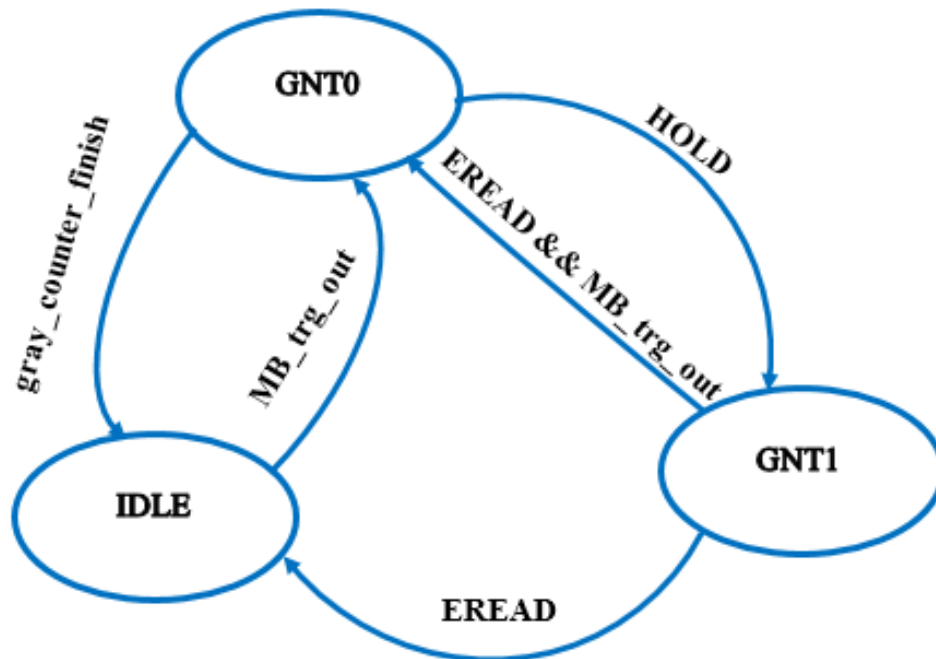
Time required to send data:

$256 / (1.6 * 10^9) = 160 \text{ ns}$



Timestamp

State diagram



States:

IDLE – idle

GNT0 –time saved, waiting for **HOLD** approval signal during T_{Hold} time

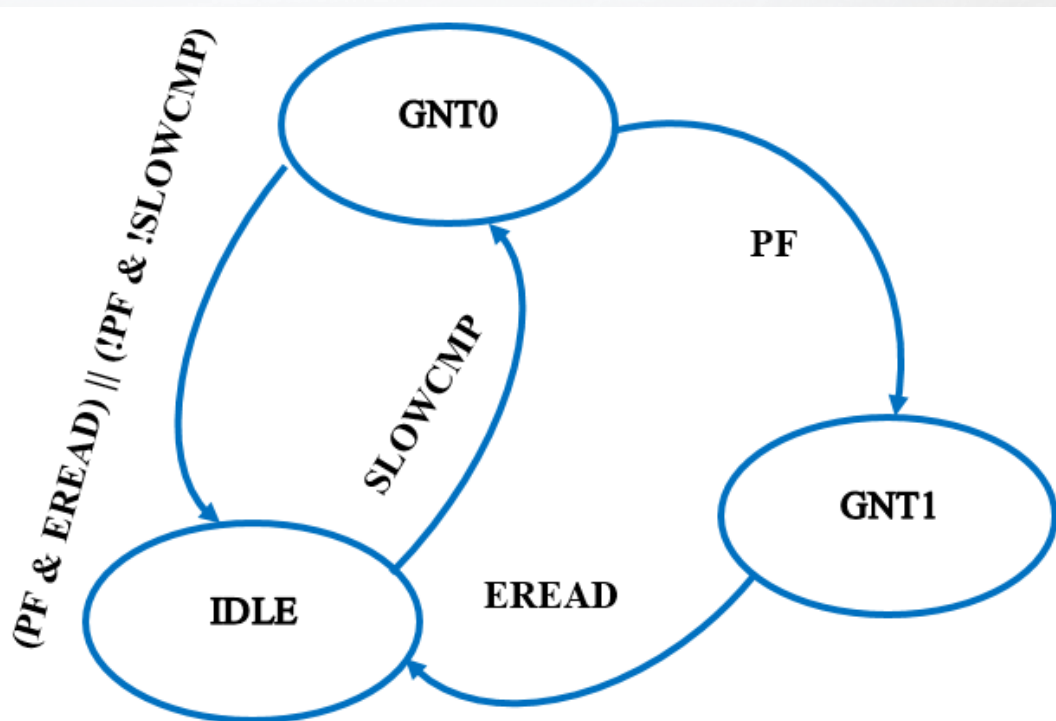
GNT1 – time saved and approved, waiting for read enable signal

Main characteristics:

- timestamp resolution – 3.125 ns
- gray code
- 14 bit

Peak detector

State diagram



States:

IDLE

GNT0 – data processing

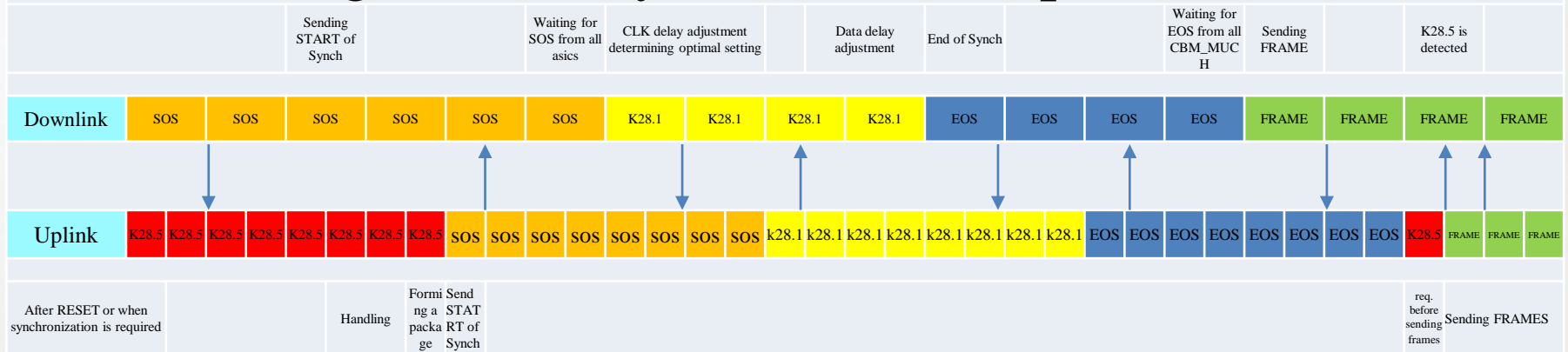
GNT1 – peak time found and saved, new incoming data is ignored, waiting for read enable signal

Main characteristics:

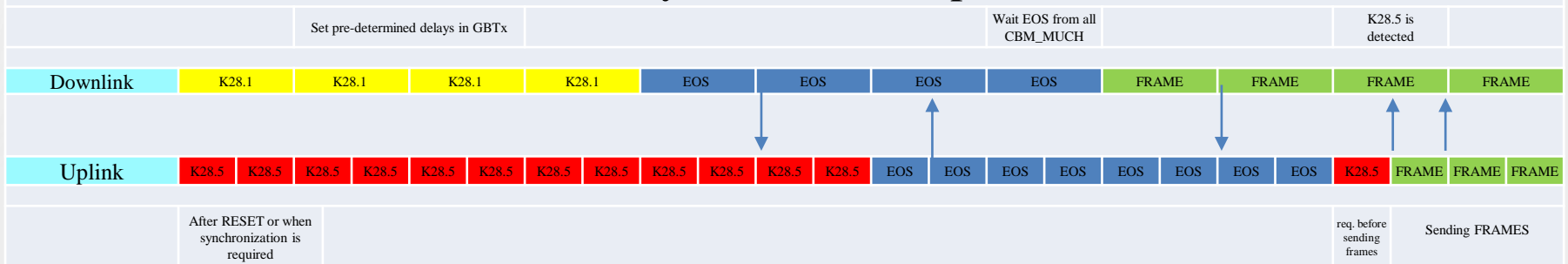
- 2 modes: simple and smart
- prevention of the false peak detection due to the noise
- adjustable sensitivity level for noise detection
- adjustable peak detection condition
- overlay detection

GBT synchronization

Regular link synchronization procedure



Quick link synchronization procedure



GBT outgoing frames

	BYTE0										BYTE1										BYTE2										BYTE3										
TYPE	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
SOS	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	
EOS	1	1	0	0	1	1	1	1	1	1	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	0	0

Not coded by the 8b10b coder

	BYTE0								BYTE1								BYTE2								BYTE3							
TYPE	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
K28.5	1	0	1	1	1	1	0	0	1	0	1	1	1	1	0	0	1	0	1	1	1	1	0	0	1	0	1	1	1	1	0	0
K28.1	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
Dummy HIT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
HIT	0	1	5 bit Number channel					S	8 bit ADC								14 bit time stamp								Res							
ACK	1	0	2 bit ACK	4 bit Sequence number				CP	4 bit status value				15 bit register content								4 bit CRC											

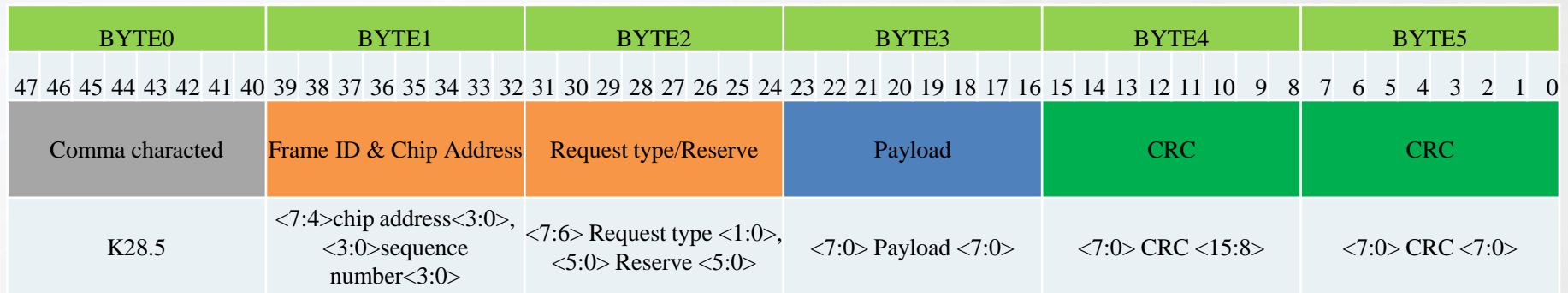
Coded by the 8b10b coder

Name	Comment
S	Overlay Pick Detector
CP	Config parity
Res	Reserve

Ack[1:0]	Comment	STATUS[3:0]	Comment
0x0	No operation	0x0	No warning
0x1	Acknowledgment	0x1	FIFO full
0x2	Error	0x2	Sync alert
0x3	Warning(See STATUS[3:0])	0x3	Sequence error
		0x4	Check register error

SOS – start of synchronization
EOS – end of synchronization
K28.5 – waiting for synchronization
K28.1 – calculated latch (control word)

GBT incoming frames



Chip Address	Comment
0x0 ... 0x7	Individual chip addressing (max 8)
0x8 ... 0xE	Reserve
0xF	Broadcast

Request Type	Code	Ack request	Payload	Comment
No_op	0x0	No	X	No operation
Wraddr	0x1	Yes	[7:0] address	Write address. Address remains for consecutive Wrddata request. But Rddata overwrites it with register address used in Rddata frame.
Wrddata	0x2	Yes	[7:0] data	Write data to register block (address set previously by Wraddr). Wrddata must have the sequence number higher by one from the last Wraddr command, otherwise it is not accepted.
RDdata	0x3	Yes	[7:0] address	Read data from register

Present status

The following items are developed:

- **Basic structure of the CFP**
- **Behavioral models of the main subblocks**
- **Functional tests**

Items to do:

- **Assembly of all subblocks**
- **More complex verification tests**
- **Layout design and verification**
- **Noise and IR-drop analyzes**

Chip submission to be done in December 2016

Thank you for Your attention!