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Analysis of noise immunity at common circuits of the front end parts of high-speed transceivers

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Noted that the work of on-board and land data transmission systems, operating at speeds of several Gbit/s and above, greatly influenced by the parasitic parameters of the internal and external connections of the chip, which leads to violation of the integrity of transmitted and received signals, including due to the effect of interference at common circuits. The method of analysis of the impact of interference on the supply lines and ground within the front-end parts of high-speed transceivers to establish a predominantly circuit macromodels with the selected nodes are affected by interference is presented. Unlike the well-known IBIS models, that contain information on I/O buffers in the tables with counts of the current-voltage characteristics and time-dependency of the output voltage, the proposed macromodels are deprived of a number of shortcomings and limitations of these models. In particular, the possibility of using macromodels are not limited to solving specific computational problems related to the analysis of signals integrity. This paper shows how to use the proposed macromodels to refine the system parameters, describing the interference of power circuits and ground, for a wide range of devices and blocks. The results of the comparison in general the alternative embodiments of high-speed transceivers at the physical layer with the use of additional noise immunity criteria are also presented.

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