

Layout-aware Soft Error Rate Estimation Technique for Integrated Circuits under the Environment with Energetic Charged Particles

Friday, 14 October 2016 14:45 (15)

This work considers the technique for modeling of multiple errors caused by charged particles in sub-100 nm devices. This technique estimates the Soft Error Rate taking into account layout of integrated circuit. Comparison of simulated data with data from experiments on testing facilities is provided.

Primary author(s) : Mr. BALBEKOV, Anton (SRISA)

Co-author(s) : Dr. GORBUNOV, Maxim (SRISA); Dr. BOBKOV, Sergey (SRISA, NRNU MEPhI)

Presenter(s) : Mr. BALBEKOV, Anton (SRISA)

Session Classification : Methods of experimental physics - parallel VI

Track Classification : Methods of experimental physics