The special radiation-hardened processors for new highly informative experiments in space

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Three basic branches

1X1:
- CMOS 0,5 мкм
- CMOS 0,35 мкм
- SOI 0,5 мкм
- SOI 0,35 мкм
- SOI 0,25 мкм

Development ASIC and board:
- Microprocessors,
- Peripheral controllers, SRAM...
- Development board, board for testing chips
- Board for GAMMA-400

Software:
- Real-time OS «Baget»
- Software for testing and debugging
Microprocessors «KOMDIV»

Fault-tolerant:
- 5890VM1T, 1900VM2T, 1907VM038, 1907VM014, 1907VM044, 1907VM028, 1907VM066,
- 1907VK016
1907VM044 system-on-chip

- 0.25 μm SOI CMOS
- 66 MHz
- KOMDIV 32-bit,
- Local TMR
- Redundant SpaceWire interface controller
- Redundant MIL STD 1553B interface
- 3 real time timers
- SRAM controller
- ROM controller
- GPIO
- 2 RS-232 controllers
- SPI
- JTAG
Fault-tolerant

- DICE-cell based cache memory
- Parity bit (1 per byte) for cache memory
- Hamming error correcting code for the built-in MIL-STD 1553 DICE-based memory
- DICE-cells in register files with Hamming code protection (13,8) hardware scrubbing
- SECDED for external memory
- Hardware possibility of using SRAM in TMR mode
- Spatial separation of neighboring bits (protection from MBU)
- “guaranteed boot” from ROM
- Local TMR
- MBIST
- TID: >200 krad (Si)
- SEL free
- 0.25 μm SOI CMOS
- is used for the connection of various switches and systems-on-chip
- 6 RapidIO ports, the transferring environment is configured independently: LP-Serial 4X or 1X
- Maximum transferring speed is 1.25 Gbit/sec (per line)
- It has the routing table for each port, performance control system, built-in error-correcting block
- The switch can directly connect up to 256 devices in the system
- Individual routing tables allows to flexibly configure the transferring of data packages.
- The performance control system is used for the defining of characteristics of data flow in channel, overload detection, the localization of locking.
System on chip – 128-bit DSP
- >2 GFLOPS @ 100 MHz
- >2 Gbit/s to external memory

Architecture:
- 32-bit control core
- 128-bit computational co-processor
- SPI, DDRII, RS232, RapidIO
Multiport switch SpaceWire with embedded processor

1907VM056

- Frequency – 100 MHz
**1907VM066**

- **SOI «Micron»**
- **Rad-hard 32-bit microprocessor with coprocessor processing and compare data image for navigation and on-board systems**
  - UCC, B: 3,3
  - Frequency, MHz: > 100
  - Power consumption @100MHz, W: < 6
  - Case CPGA: 407 pins
Fault-tolerant microcontroller with TMR
- Processor 100 МГц
- SRAM 2 MB with correction
- FPGA 50 000 gates
Developing boards

- Central processor unit for SSNI “GAMMA-400” based on 1907VM038
- Control unit for SSNI “GAMMA-400” based on 1907VM044
- Switch Serial RapidIO based on 1907KX018 for OpenVPX systems
- Switch SpaceWire based on 1907VM056 for OpenVPX systems
- Central processor unit based on 1907VM028 for OpenVPX systems
- Central processor unit based on 1907BM066 in form factor PC-104
- Peripheral module with interface 1533B in form factor PC-104
- Performance central processor board:
  - Based on 1907BM028 – 0,1 Gops на 64-bit operand
  - Based on 1907BM038 – up to 2 GFlops на 32-bit operand
- Performance computer up to 2-8 GFlops on 32-bit operand
- Throughput interprocessor channels:
  - Up to 6 channels Serial RapidIO, 1 Gbit/s; up to 6 channels SPACEWIRE, 200 Mbit/s;
THANK YOU

FOR YOUR ATTENTION