

5 bit current steering low power DAC for threshold voltage adjustmen

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A low power area efficient 5 bit current steering DAC is presented. The proposed DAC is integrated to prototype the readout channel for muon chamber in CBM experiment. DAC was implemented with an area of 0.019 mm² in the CMOS process using UMS MMRF 180 nm technology. This DAC has ultralow power consumption - 25μW. The measured differential nonlinearity (DNL) is better than 0.25 LSB, integral nonlinearity (INL) is better than 0.2 LSB. In this paper the main steps of design flow, simulation results and measurement results are presented.

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