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Complex function block of a low-power digital peak detector with input disturbance correction

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A low-power digital peak detector, intended for use in a 32-channel IC, reading out and processing the signals of the FAIR accelerator detectors of the CBM experiment, is considered. In compare with its analogues the peak detector (PD) has been added by an option of correcting input disturbances, which may be digitized by on ADC. The block has been designed for operation with an 8-bit ADC, placed in the IC's readout channel and having the following characteristics: power consumption 0.46 mW, occupied area 115 x 115 mm2, operation frequency of 50 MHz. Due to its efficient parameters on power consumption and occupied areas the given block meets the requirements, set to the CBM electronics, and will be included in the 32-channel IC for reading out the GEM detector signals, which is under development in MEPhI ASIC LAB. The PD block is implemented by the 180nm CMOS technology of UMC (Taiwan).

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