Development and tests of the 100 ps FPGA-based TDC readout board for high granular time-of-flight neutron detector at BM@N experiment.

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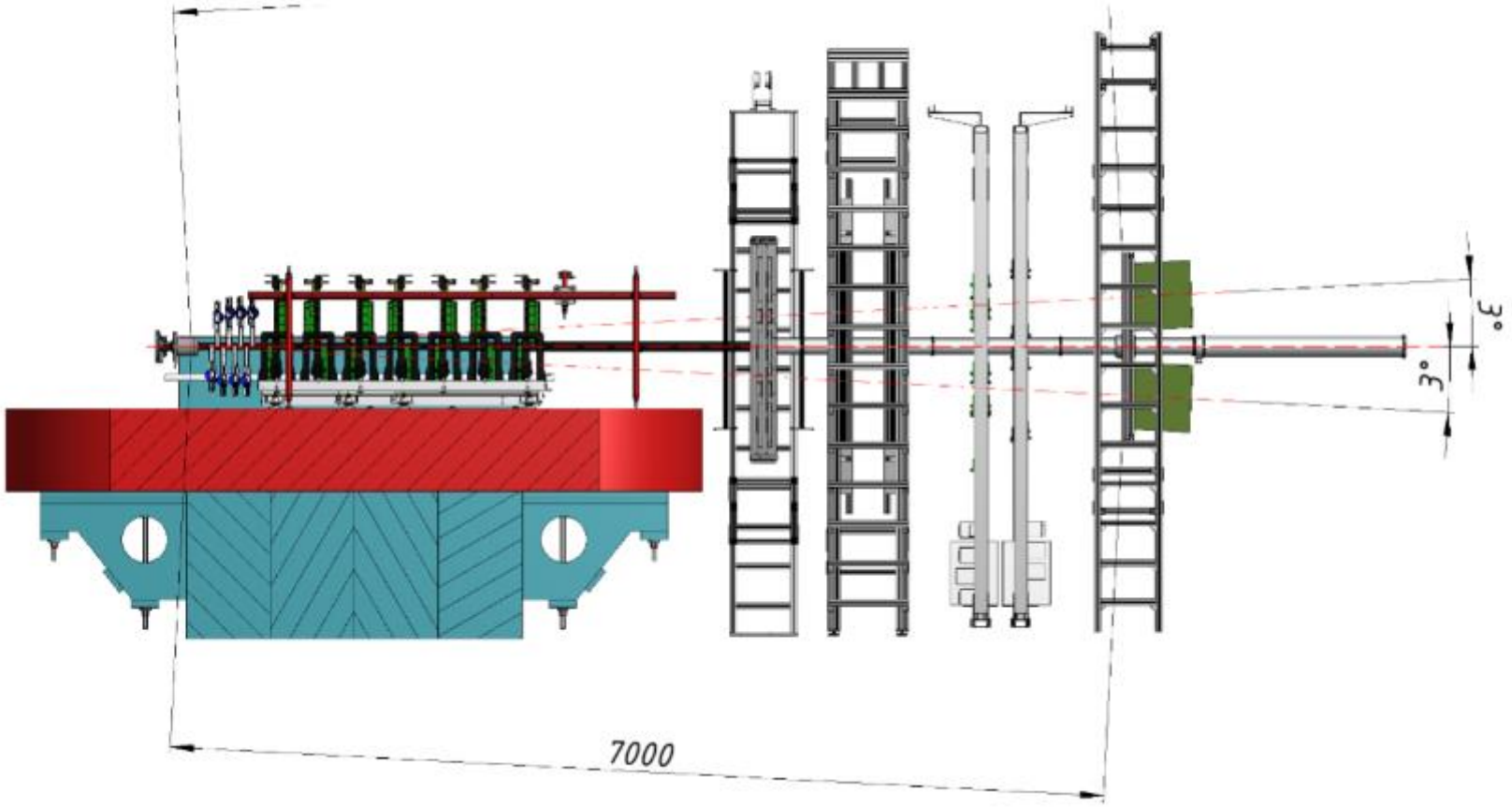
Acknowledgements:
This work was carried out at the Institute for Nuclear Research, Russian Academy of Sciences, and supported by the Russian Scientific Foundation grant №22-12-00132.

Outline

- HGND readout topology
- 100ps FPGA based TDC
- Status of the FPGA firmware development
- Status of the readout board development
- Status of the DCS & readout software architecture

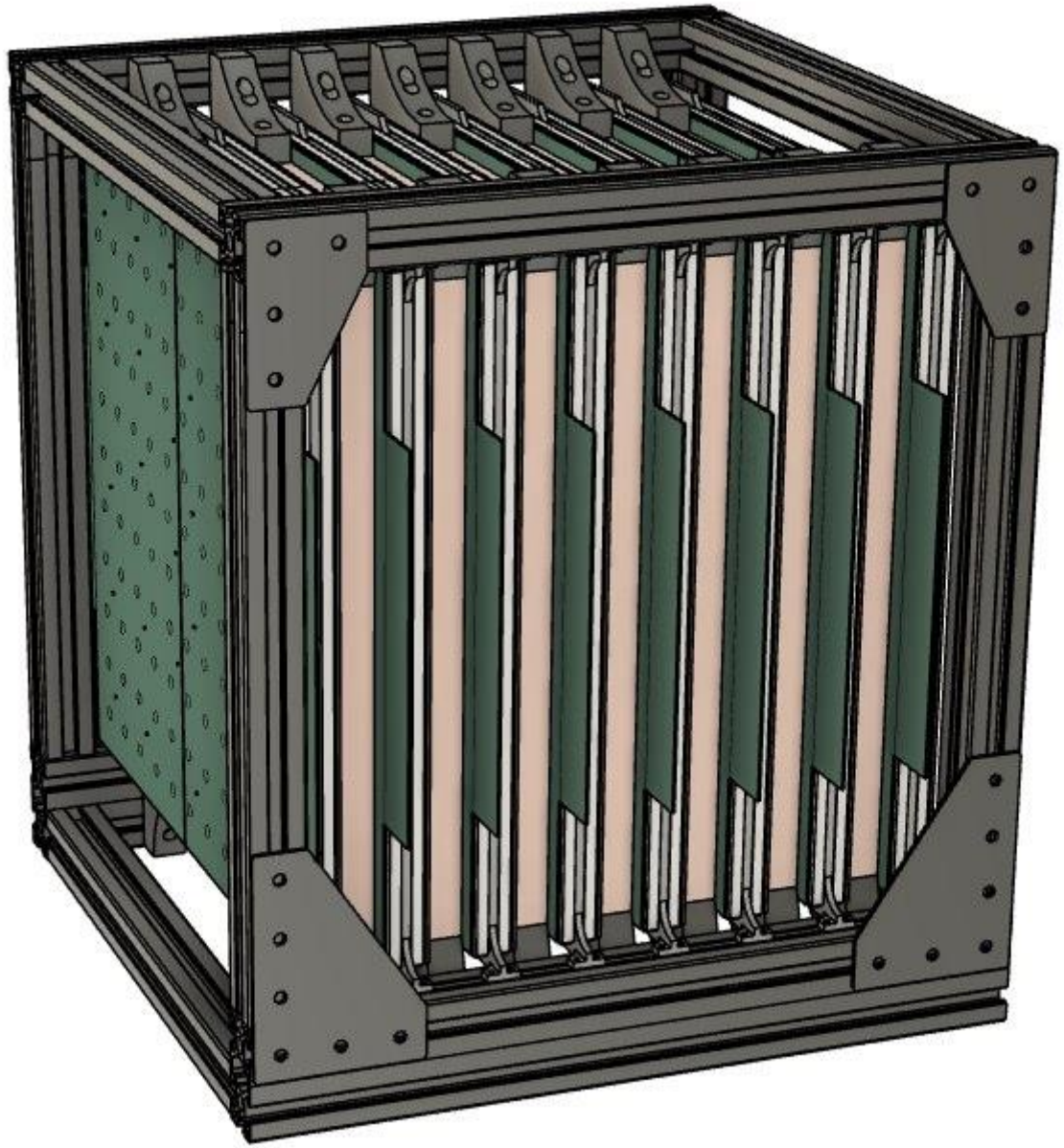
Detector arrangement

- Detector for high-energy neutron flow measurement
- ToF method with T0 as the “start” signal source
- 7m measurement distance
- Detector is split into 2 “blocks” for improved acceptance



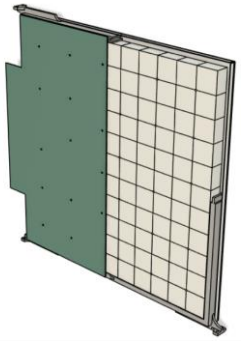
Detector “block”

- Each block consists of:
  - A VETO-layer
  - 8 Cu absorbers
  - 8 sensitive layers
    - 11x11 grid of scintillatiors each
- Assembly is light-tight and air-cooled
- Framing is built with light-weight Al profiles

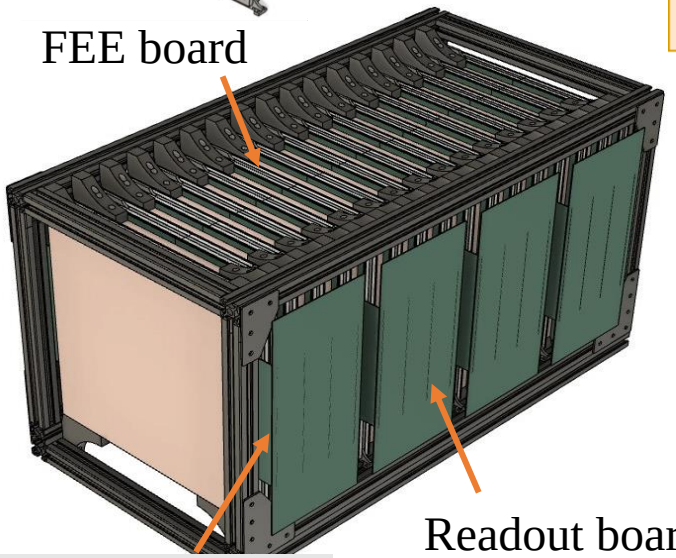


FEE & readout architecture

- 16 layers with scintillation matrix 11X11
- 16 LED boards
- 32 FEE boards
- 8 Readout boards
- 3 FPGA per board
- 84 channels per FPGA
- 2000 channels in total

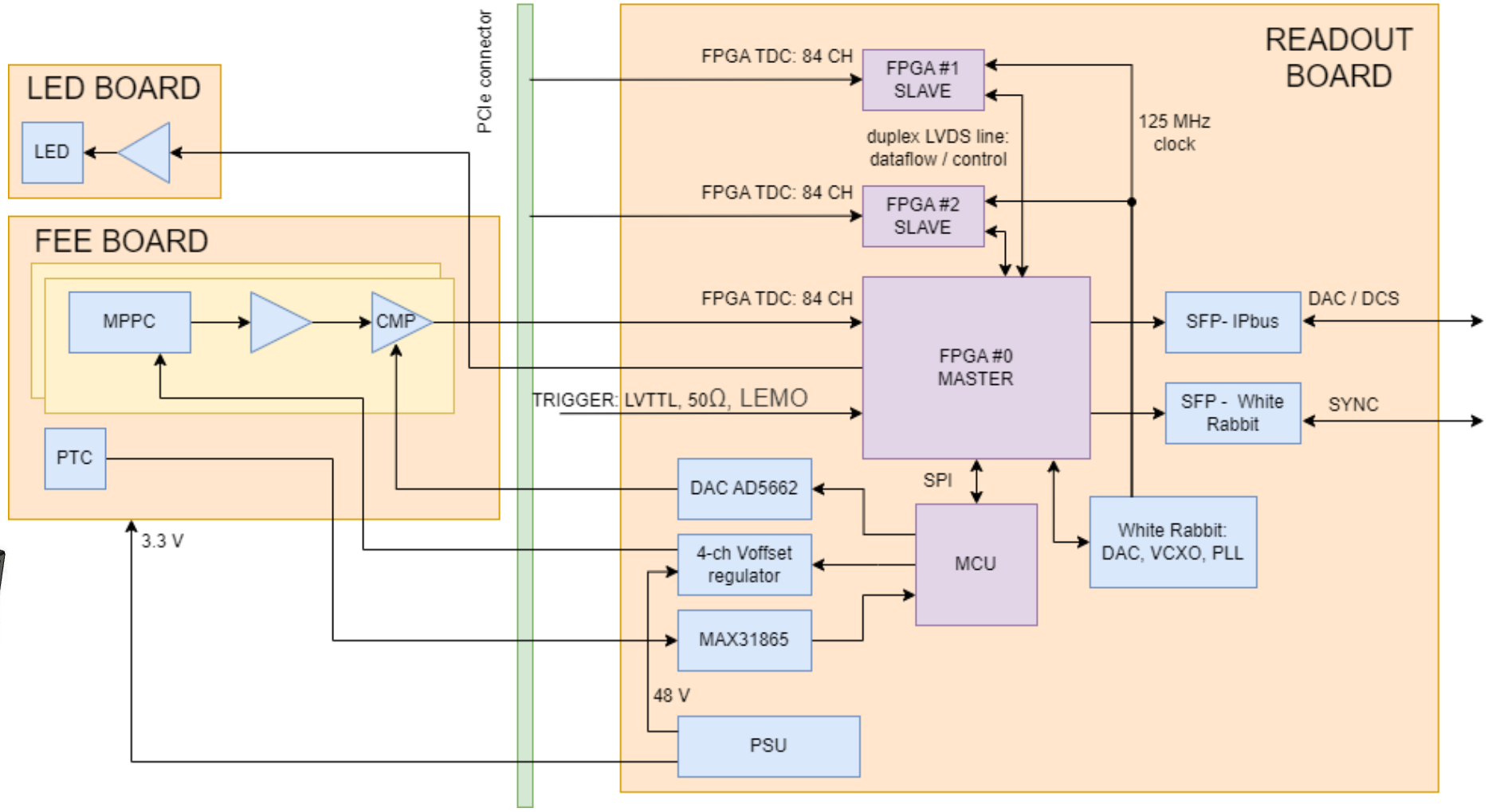


FEE board



Readout board

PCIe connector



Readout & trigger

- ***100 ps*** TDC is implemented in Kintex 7 FPGA, 84 channels per FPGA chip (2000 total)
- ***White Rabbit*** (WR) is used for event's time synchronization (8 links total):
  - TDCs use clock sourced from WR synchronous to whole BM@N
  - WR timestamps are assigned to measured events

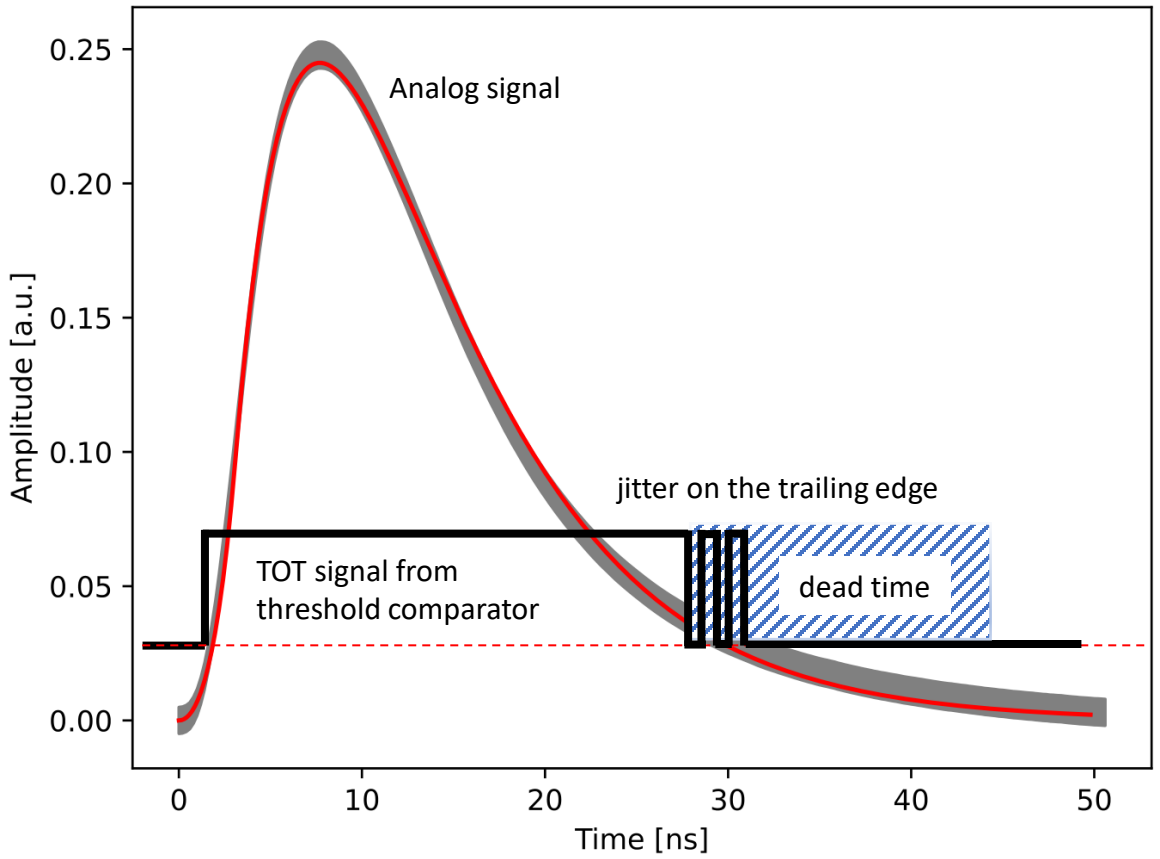
- Ethernet UDP protocol (***IPbus*** [1]) is used for data forwarding and board control
- Local network connect readout boards (8 ethernet links) with FLP

- The maximum HGND channel load is 3 kHz. The event size is 7x16 bits. The upper limit per link is not exceed ***100 Mbit/s***. ***The continuous readout*** is implemented without busy signal.

- The trigger is processed on FLP site:
  - Trigger signal is connected to TDC channel and digitized with WR timestamp in FPGA
  - Message trigger accompanied by a timestamp is transmitted to FLP for event selection

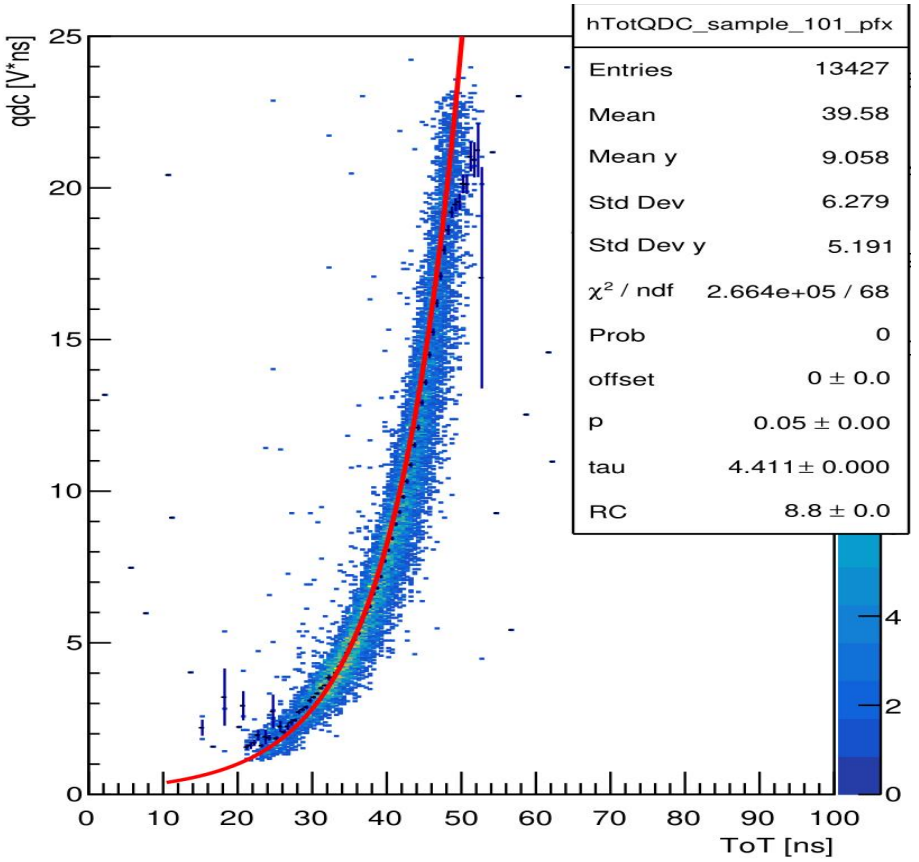
[1] C. Ghabrous Larrea, K. Harder, D. Newbold, D. Sankey, A. Rose, A. Thea and T. Williams, ***IPbus: a flexible Ethernet-based control system for xTCA hardware***, *JINST 10 (2015) no.02, C02019.*

TDC Time Over Threshold (TOT)



- The threshold is tunable around 20 mV
- Signals length range is 20 – 60 ns
- Signals less than 6.4 ns are rejected for noise reduction
- Dead time is tunable in range 30 – 200 ns for comparator jitter filtering
- Minimum TOT time and dead time available in FPGA TDC are 3.2 ns

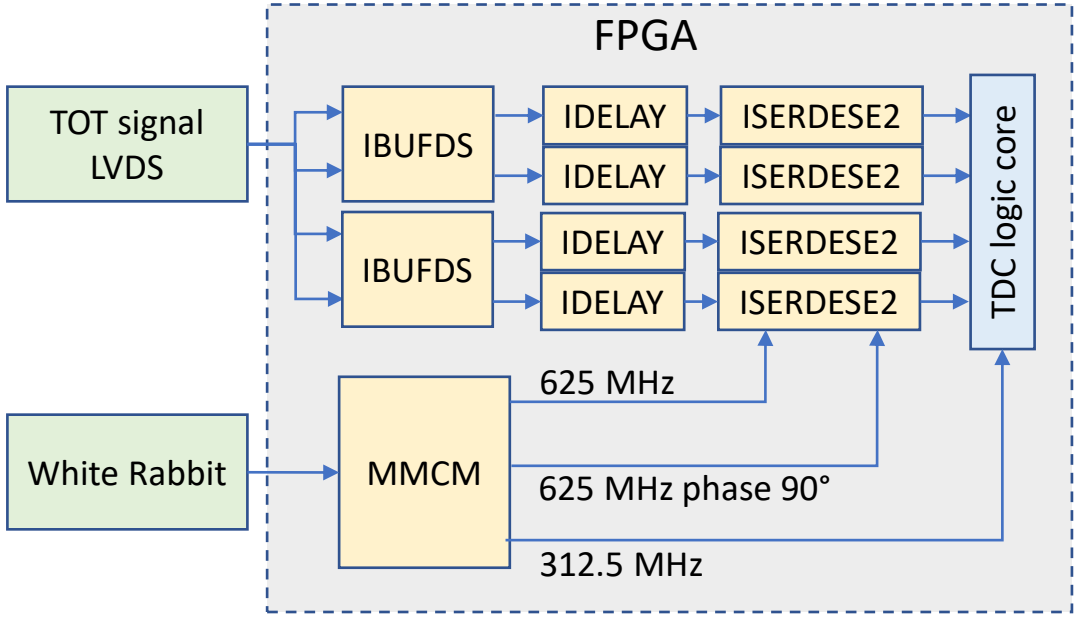
Amplitudes vs TOT time with analytical forecast

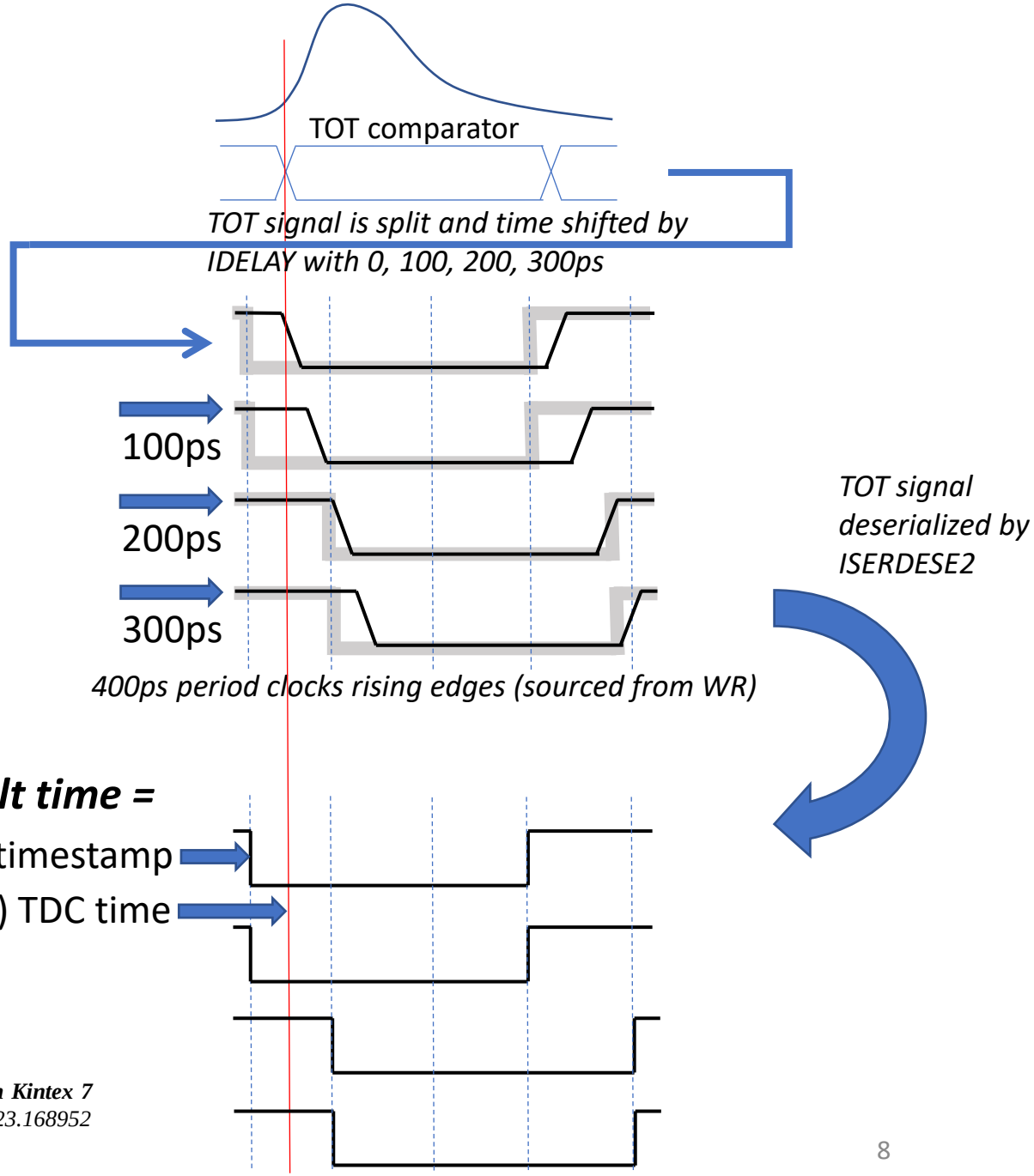


- TOT amplitude resolution is in range 14 - 22%
- Is used for time slewing correction

[2] N. Karpushkin, D. Finogeev, F. Guber, D. Lyapin, A. Makhnev et al., ***Analytical description of the time-over-threshold method based on time properties of plastic scintillators equipped with silicon photomultipliers,*** *DOI: 10.1016/j.nima.2024.169739*

The 100ps FPGA TDC principle of operation



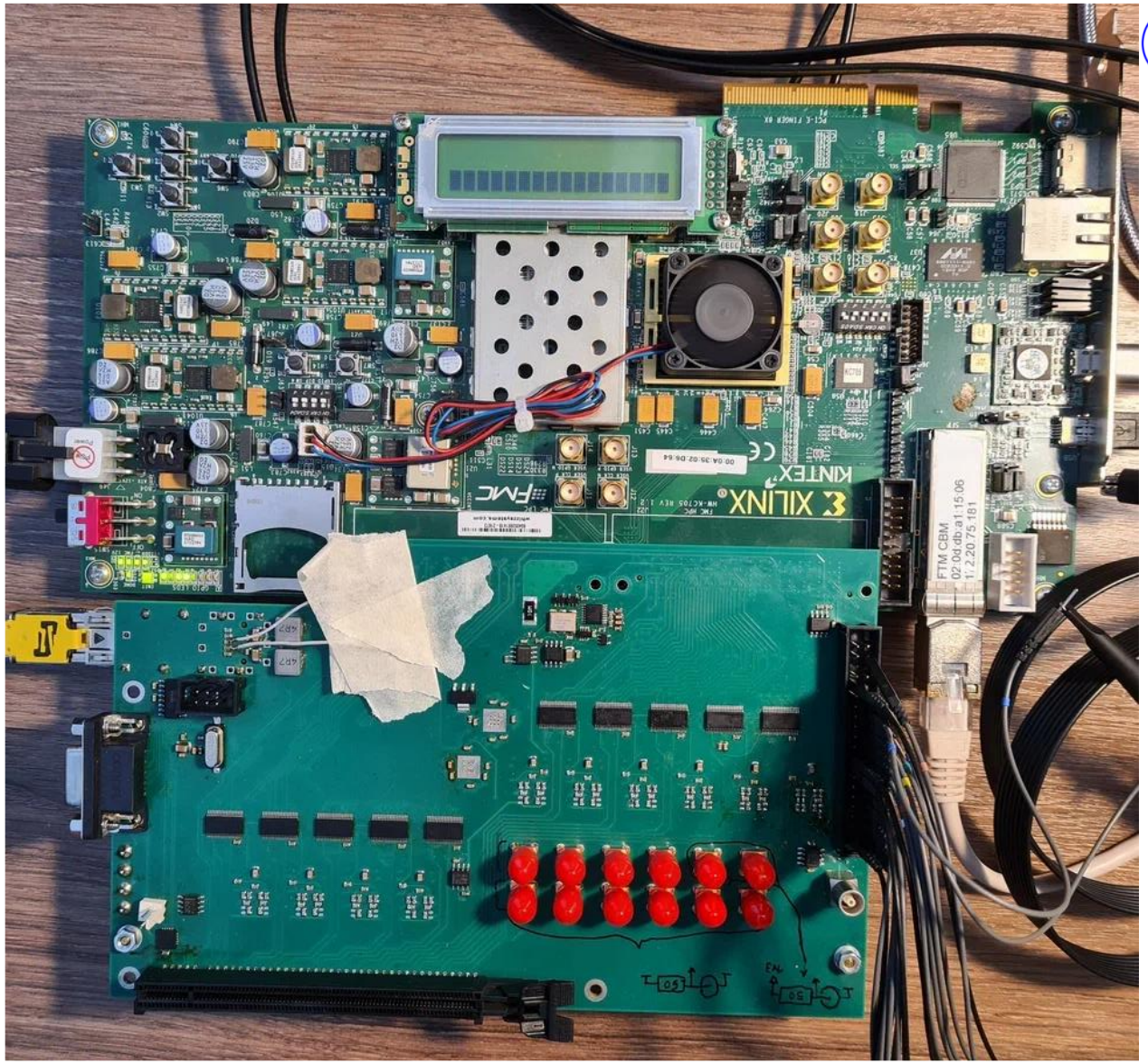


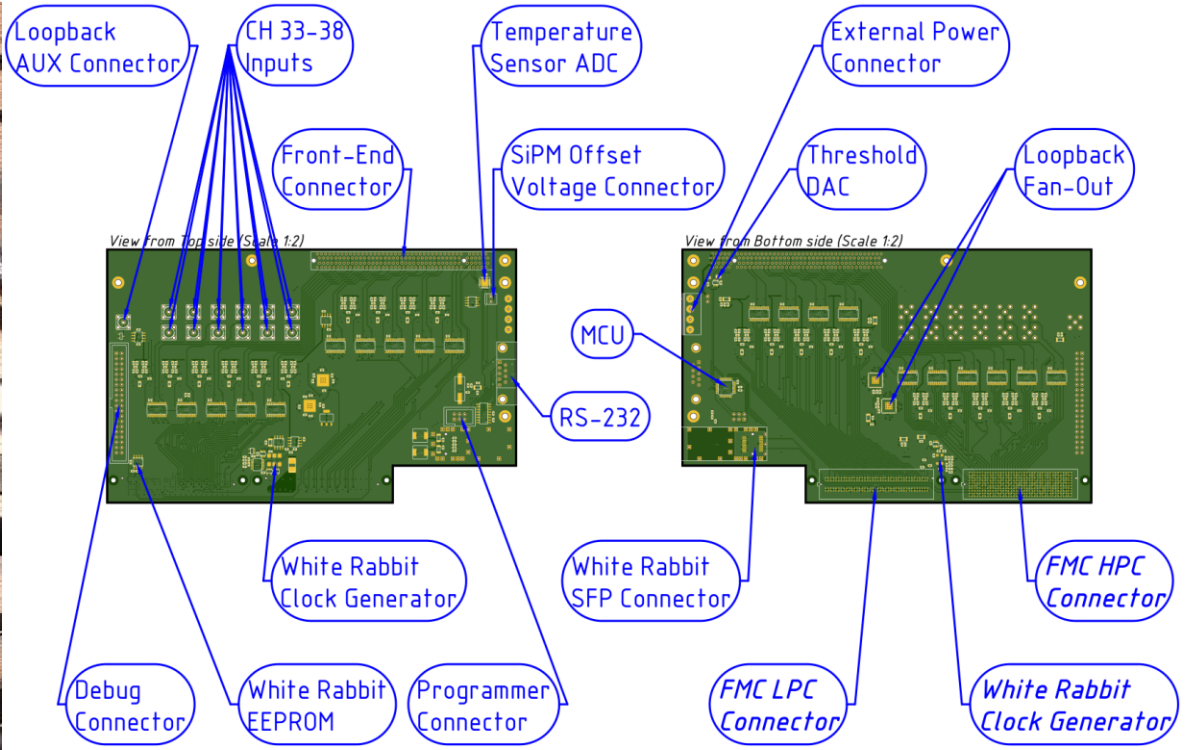
The TDC is **based on the Kintex-7** input serial-to-parallel converter with oversampling capability and programmable delay. The design is **based on Xilinx recommendations**, and uses **only documented features** of the FPGA within its specifications.

[3] D. Finogeev, F. Guber, A. Izvestnyy, N. Karpushkin, A. Makhnev et al., ***Development of 100 ps TDC based on Kintex 7 FPGA for the High Granular Neutron Time-of-Flight detector for the BM@N experiment,*** *DOI: 10.1016/j.nima.2023.168952*

HGND readout v2 prototype (39 channels)

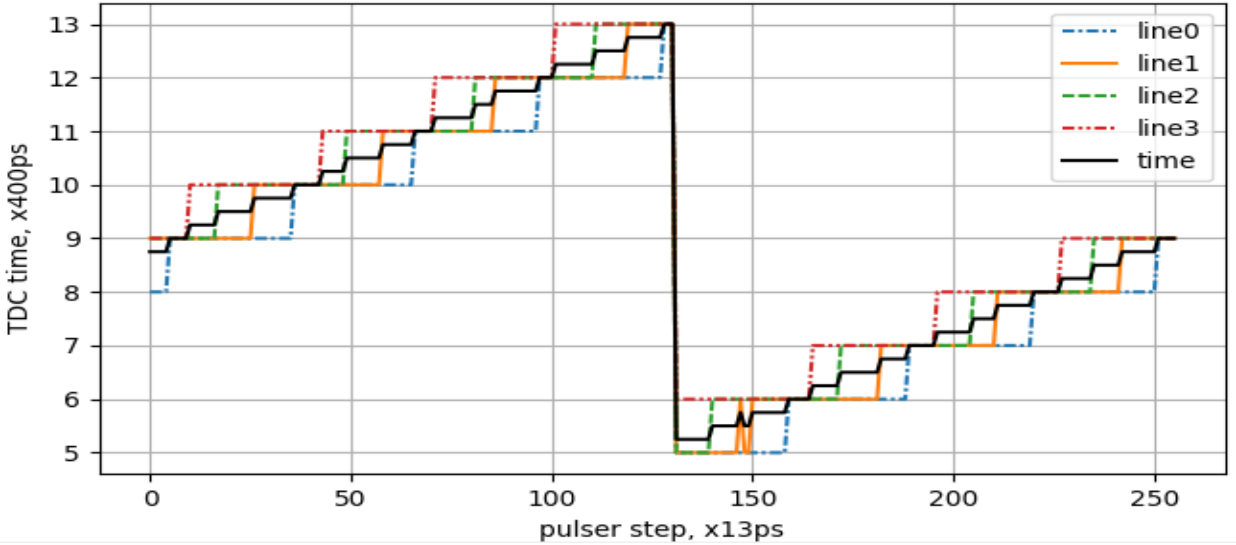
based on the Kintex 7 evaluation board (KC705)



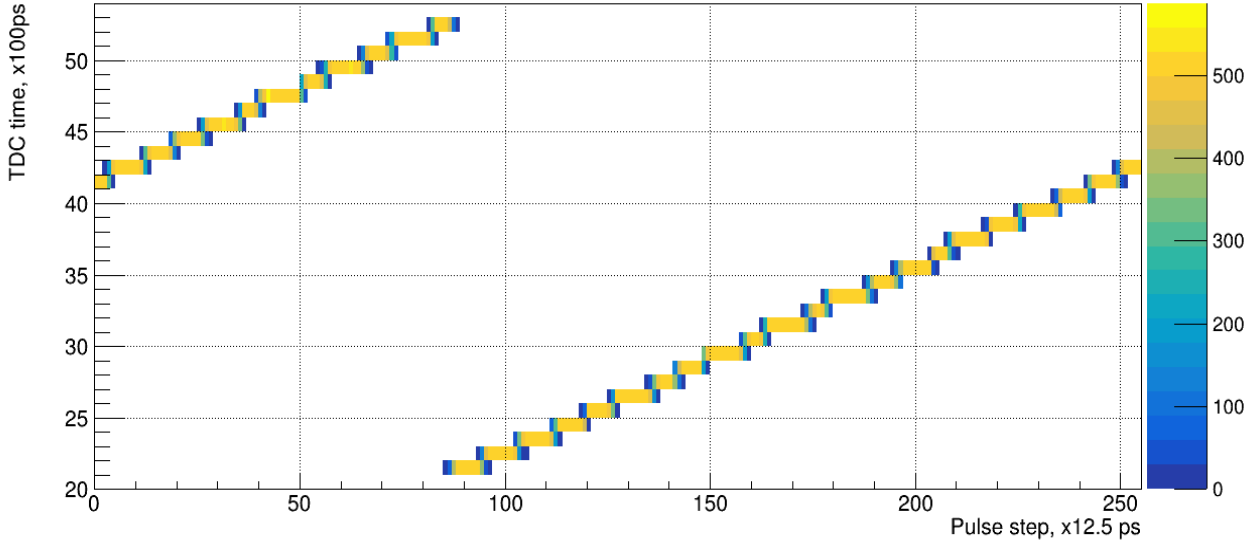


- Addon for Kintex 7 evaluation board
- 33 PCIe + 6 SMA TDC channels
- Ethernet readout
- White Rabbit synchronization
- FPGA loopback for TDC calibration
- Readout board functionality:
  - *PCIe connector for* scintillation matrix*, Temperature sensor, SiPM offset voltage control DAC threshold*

The FPGA TDC time scan results



Four TDC lines and the resulting time dependence on the pulse time shift are shown. Pulses are generated by FPGA MMCM synchronously to the TDC clock with a phase step of 12.9ps. The single scan pass was taken with a digital FPGA logic analyzer.

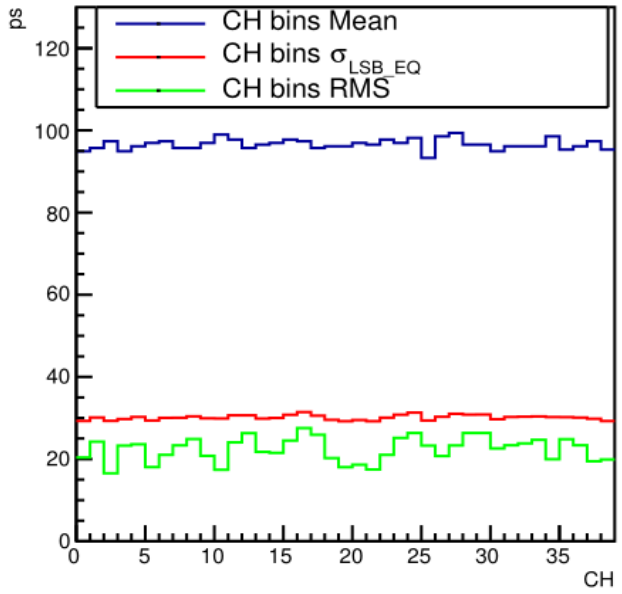


The TDC time dependence on pulse time shift. Pulses are generated by FPGA MMCM synchronous to TDC clock, and the time step is 12.9 ps. Data was taken with PC readout, 1000 events per single time shift step.

The FPGA TDC test results

PROTO_V2

TDC bins with for all 39 channels: mean value, RMS, equivalent LSB precision. Calculated with synchronous scan



The equivalent LSB precision is ~30ps.

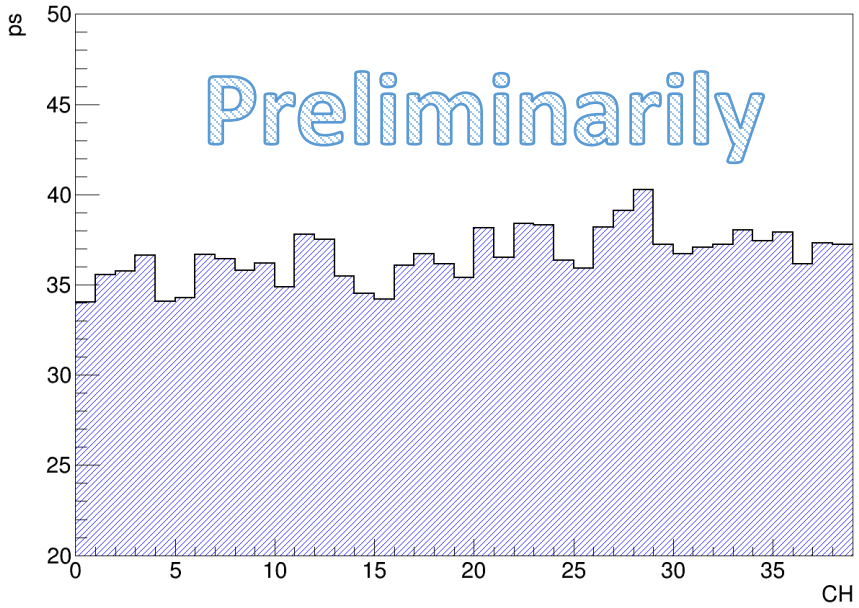
$$LSB_{EQ} = \sqrt{\frac{1}{\sum_{i=0}^{i=N-1} BinWidth[i]} \cdot \sum_{i=0}^{i=N-1} BinWidth^3[i]}$$

$$\sigma_{LSB\_EQ} = {LSB_{EQ}}/{\sqrt{12}}; \begin{cases} BinWidth[\forall i] = 100ps \\ \sigma_{LSB\_EQ} = 29ps \end{cases}$$

[4] N. Lusardi et al., "Quantization noise in non-homogeneous calibration table of a tcd implemented in fpga," DOI:10.1109/NSSMIC.2014.7431149

PROTO_V2

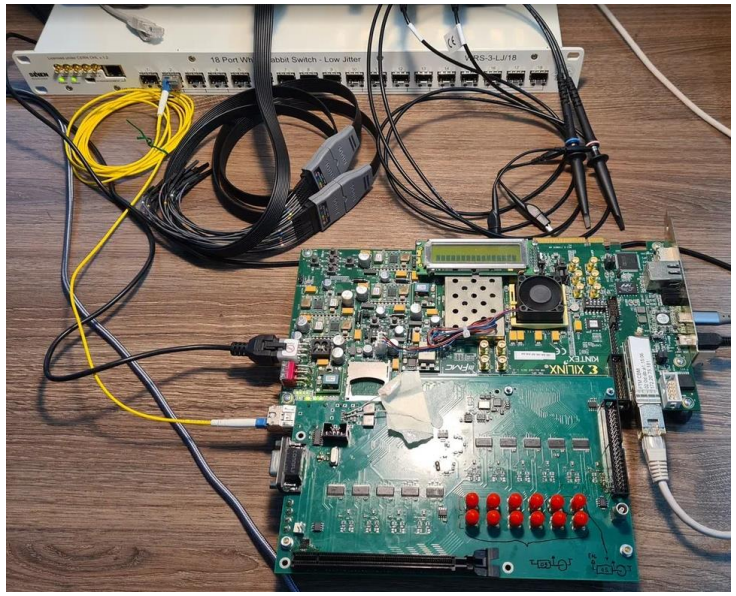
TDC bins precision measured with pulse length 101.2ns



The measured TDC precision is 35 – 40 ps.

The time resolution of the scintillation cell is 130 ps

HGND White Rabbit synchronization



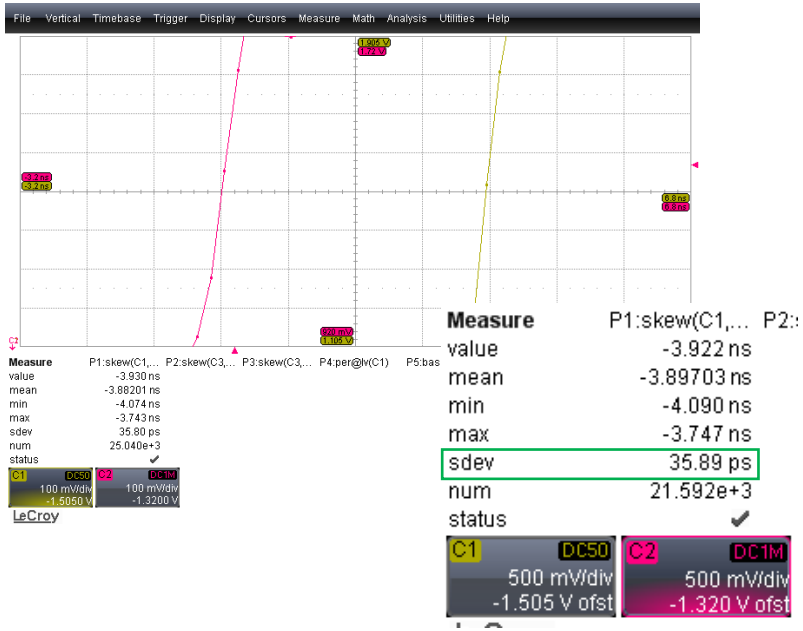
HGND WR test setup at INR
(Moscow) with provided WR switch

```
WR PTP Core Sync Monitor wrpc-v4.2-19-g54d3079
Esc = exit

TAI Time:                   Thu, Oct 3, 2024, 10:55:12

Link status:
wru1: Link up   (RX: 106, TX: 45) IPv4: 192.168.1.5 (static assignment)
Mode: WR Slave   Locked Calibrated

PTP status: slave

Synchronization status:
Servo state:                TRACK_PHASE
Phase tracking:             ON
Aux clock 0 status:         enabled

Timing parameters:
Round-trip time (mu):                910354 ps
Master-slave delay:                  442861 ps
Master PHY delays:          TX:      220857 ps, RX:     245547 ps
Slave PHY delays:           TX:           0 ps, RX:          0 ps
Total link asymmetry:                 24632 ps
Cable rtt delay:                     443950 ps
Clock offset:                             4 ps
Phase setpoint:                       10358 ps
Skew:                                     1 ps
Update counter:                          13
wrc#
```

HGND WR node monitor

PRELIMINARILY:

Clock sync jitter ~35ps (measure on FPGA output buffers)

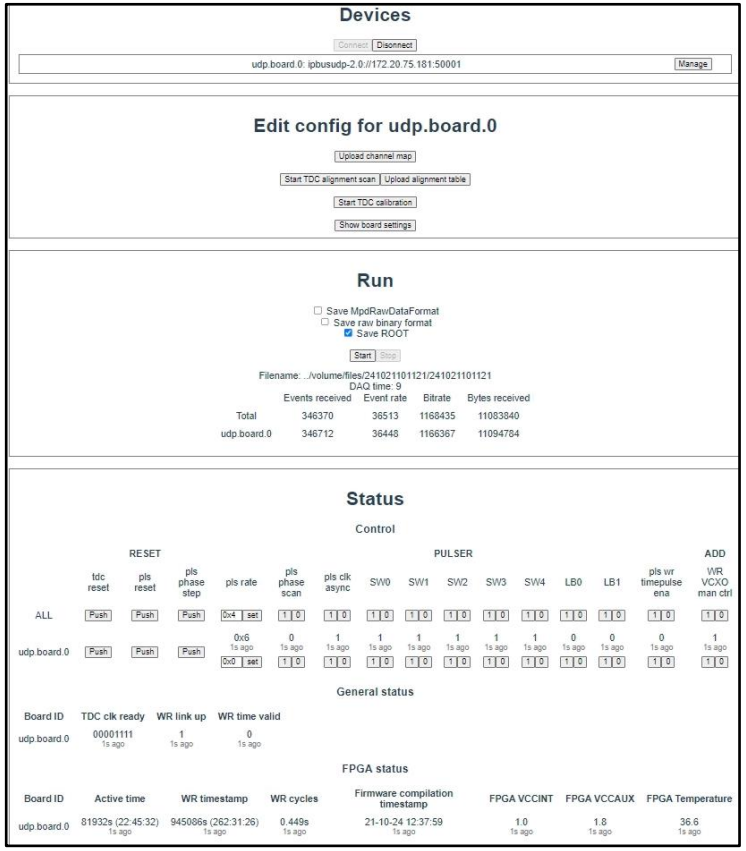


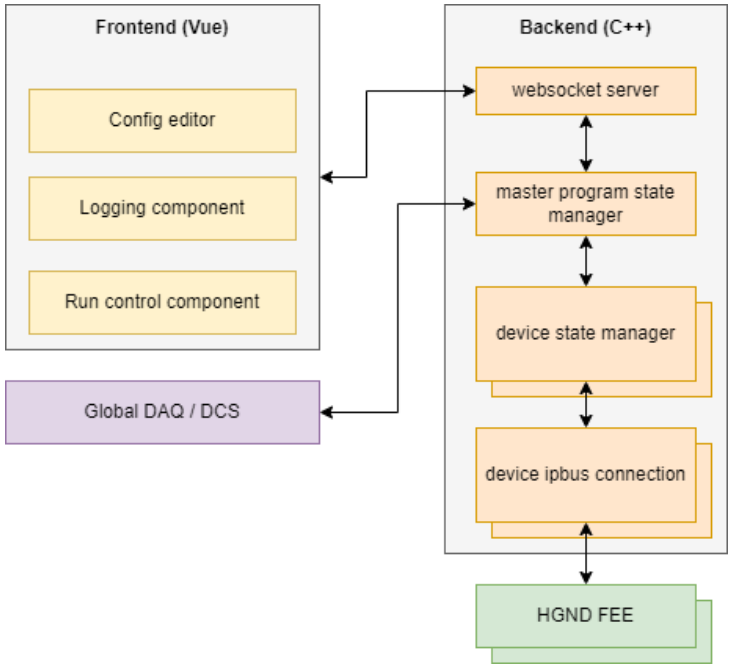
WR synchronization works:

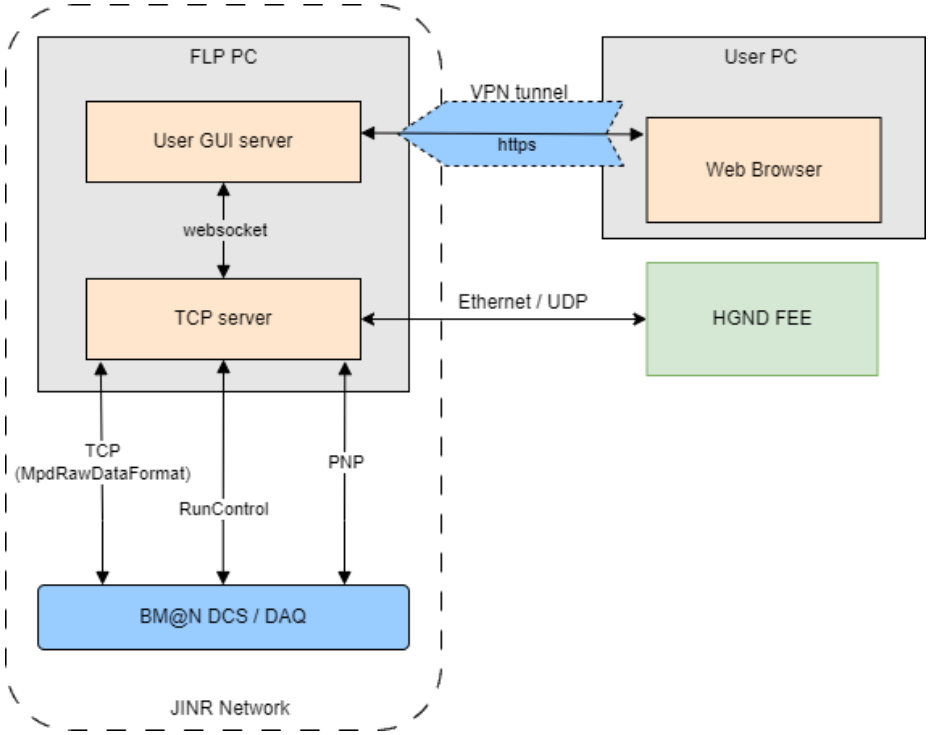
- ✓ WR switch connected
- ✓ The issue reason was wrong FIFO instance file version (for Virtex 6)
- ❑ WR design update to the latest v5.0 (optional)

Thanks to Andrey Shchipunov for help

HGND readout & DCS readout test setup







- The backend is a C++ server running on a DCS computer in the same network with detectors providing write/read operations to the detectors via an IPBus connection to the control and data acquisition board.
- Frontend is the web interface accessed via websocket.
- The interface can be run either on the DCS computer or on the operator's computer, provided that the port is available.

Performed tests:

- ✓ 400 Mbit/s data readout per board (100 Mbit is required)
- ✓ 800 Mbit/s readout rate with 2 boards was achieved (is the estimated rate for HGND with 8 links)
- ✓ Data sorting by trigger selection with two links readout: data rate 2.6 MHz (10 kHz/channel), trigger rate 10kHz.
- ✓ Data flow (soft emu) & DCS commands test on BM@N FLP
- ✓ Ready for first cosmic runs

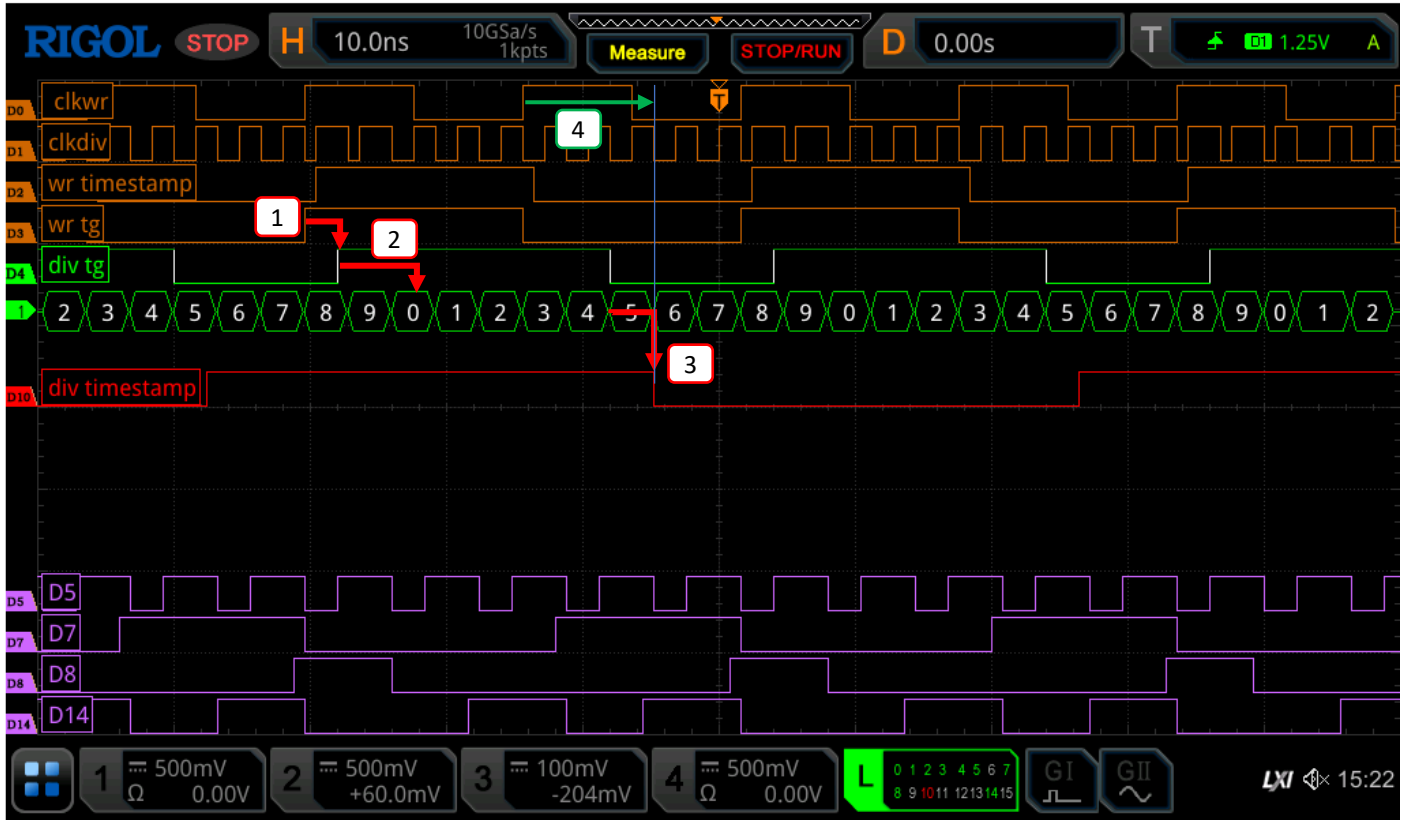
Conclusions

- Status of the HGND readout development:
  - ✓ Basic TDC tests was performed with 33 channels prototype
  - ✓ The White Rabbit synchronization works
  - ✓ Readout & DCS software is ready (basic)
  - ➢ Continue tests with prototype v2 (cosmic and beam tests with matrix, TDC development)
  - ➢ Working on the FPGA firmware: TDC revision
  - ➢ Working on the design of the full scale readout board: board routing
  - ➢ Software debugging and updates

Thank you for your attention!

BACKUP

White Rabbit timestamp synchronization with FPGA TDC



WR clock 62.5 MHz -> TDC fabric clock 312.5 MHz

- Clocks are symphonious but phase shifted
- Clock frequencies ration is 5

1. WR clock toggle signal cross clocks domain
2. Counter 0 .. 9 starts by crossed toggle signal
3. WR timestamp cross clocks domain by counter
4. WR timestamp is latched by TDC fabric clock in stable range (falling edge) of WR clock

TDC HIT timestamp format:

rejected (available in status REG)

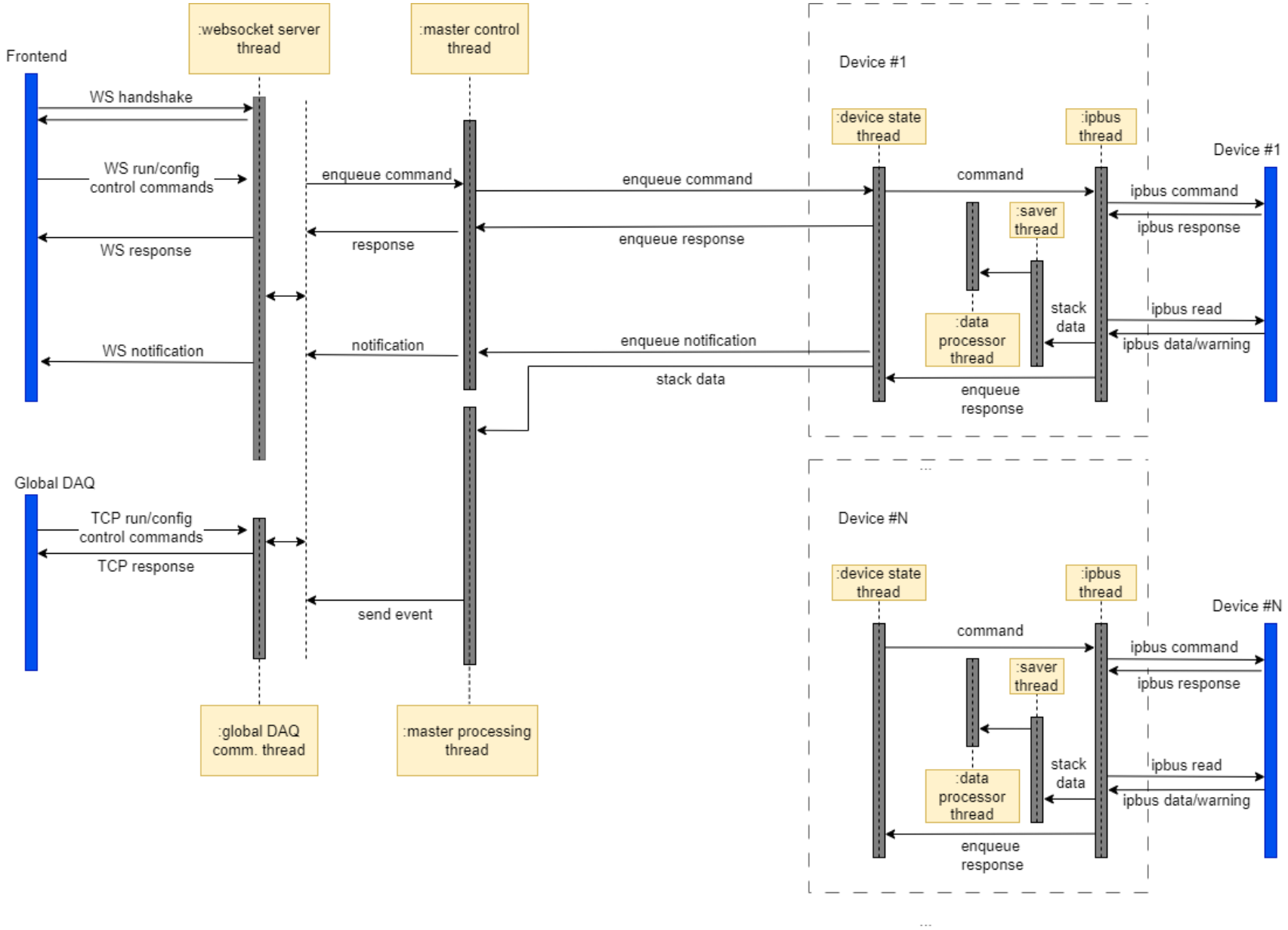
64 bit event timestamp

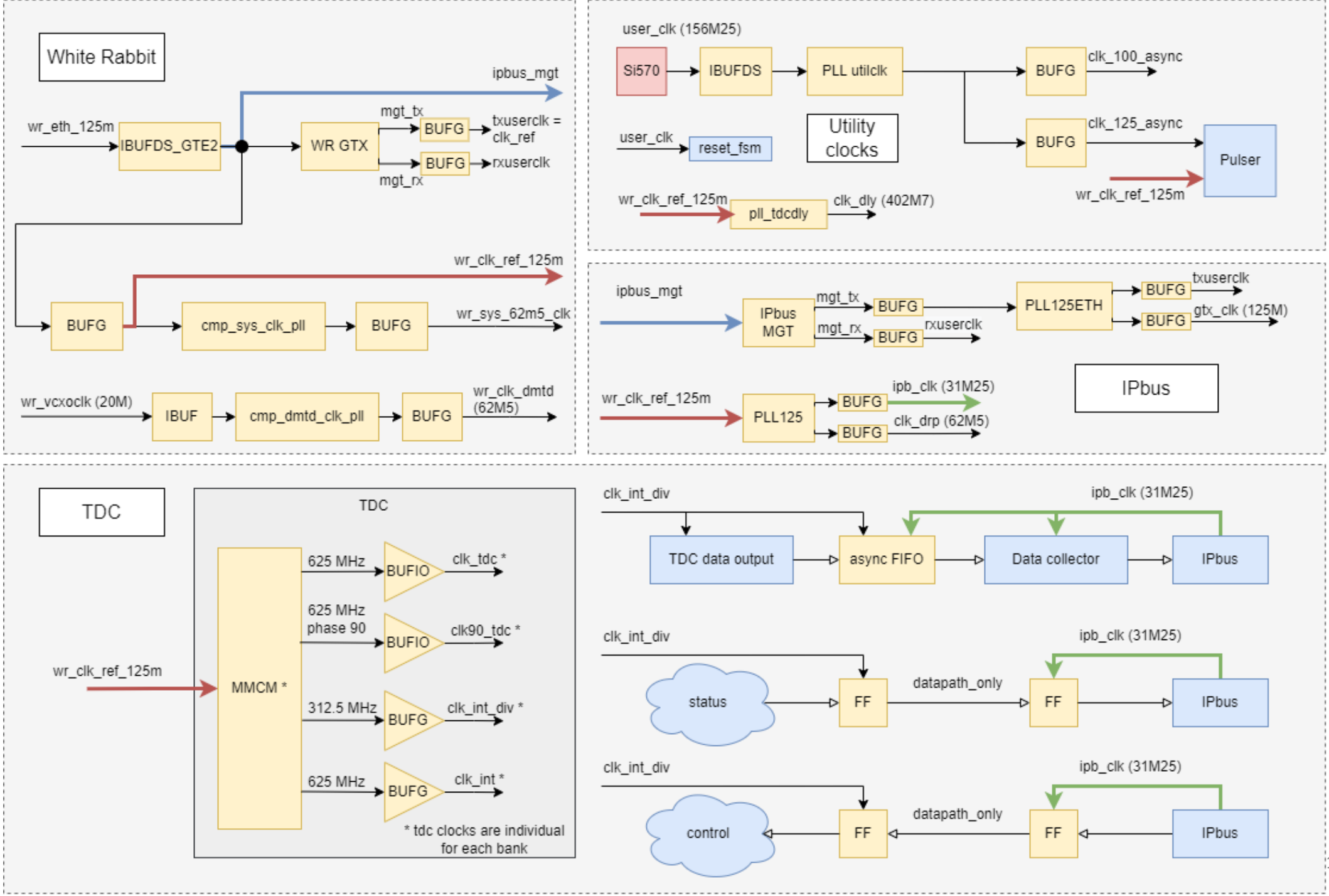
HIT rising / falling edges + pulse length 16 bit

timestamp bits: 63 | 31 | 30 | 4 | 3 | 0

WR tai [39 .. 33]	WR tai [32 .. 0]	WR cycles [27 .. 1]	TDC counter [3 ..0]	TDC time [4 .. 0]
7 MSB WR tai (centuries)	WR tai (1 sec)	WR counter/2 (32ns)	TDC fabric counter 0 ..9 (3.2 ns)	TDC fine time (100 ps)

The threading scheme of a C++ backend




White Rabbit
ipbus_mgt
wr_eth_125m
IBUFDS_GTE2
WR GTX
mgt_tx
BUFG
txuserclk = clk_ref
BUFG
rxuserclk
mgt_rx
wr_clk_ref_125m
BUFG
cmp_sys_clk_pll
BUFG
wr_sys_62m5_clk
wr_vcxoclk (20M)
IBUF
cmp_dmtd_clk_pll
BUFG
wr_clk_dmtd (62M5)
user_clk (156M25)
Si570
IBUFDS
PLL utilclk
BUFG
clk_100_async
user_clk
reset_fsm
Utility clocks
BUFG
clk_125_async
Pulser
wr_clk_ref_125m
wr_clk_ref_125m
pll_tdcdly
clk_dly (402M7)
ipbus_mgt
IPbus MGT
mgt_tx
BUFG
mgt_rx
BUFG
rxuserclk
PLL125ETH
BUFG
txuserclk
BUFG
gtx_clk (125M)
IPbus
wr_clk_ref_125m
PLL125
BUFG
ipb_clk (31M25)
BUFG
clk_drp (62M5)
TDC
TDC
wr_clk_ref_125m
MMCM *
625 MHz
BUFIO
clk_tdc *
625 MHz phase 90
BUFIO
clk90_tdc *
312.5 MHz
BUFG
clk_int_div *
625 MHz
BUFG
clk_int *
* tdc clocks are individual for each bank
clk_int_div
ipb_clk (31M25)
TDC data output
async FIFO
Data collector
IPbus
clk_int_div
ipb_clk (31M25)
status
FF
datapath_only
FF
IPbus
clk_int_div
ipb_clk (31M25)
control
FF
datapath_only
FF
IPbus